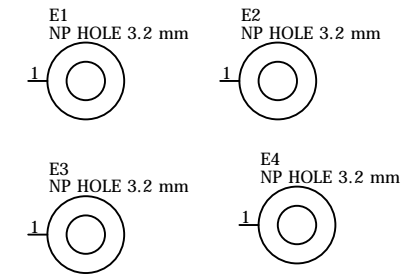
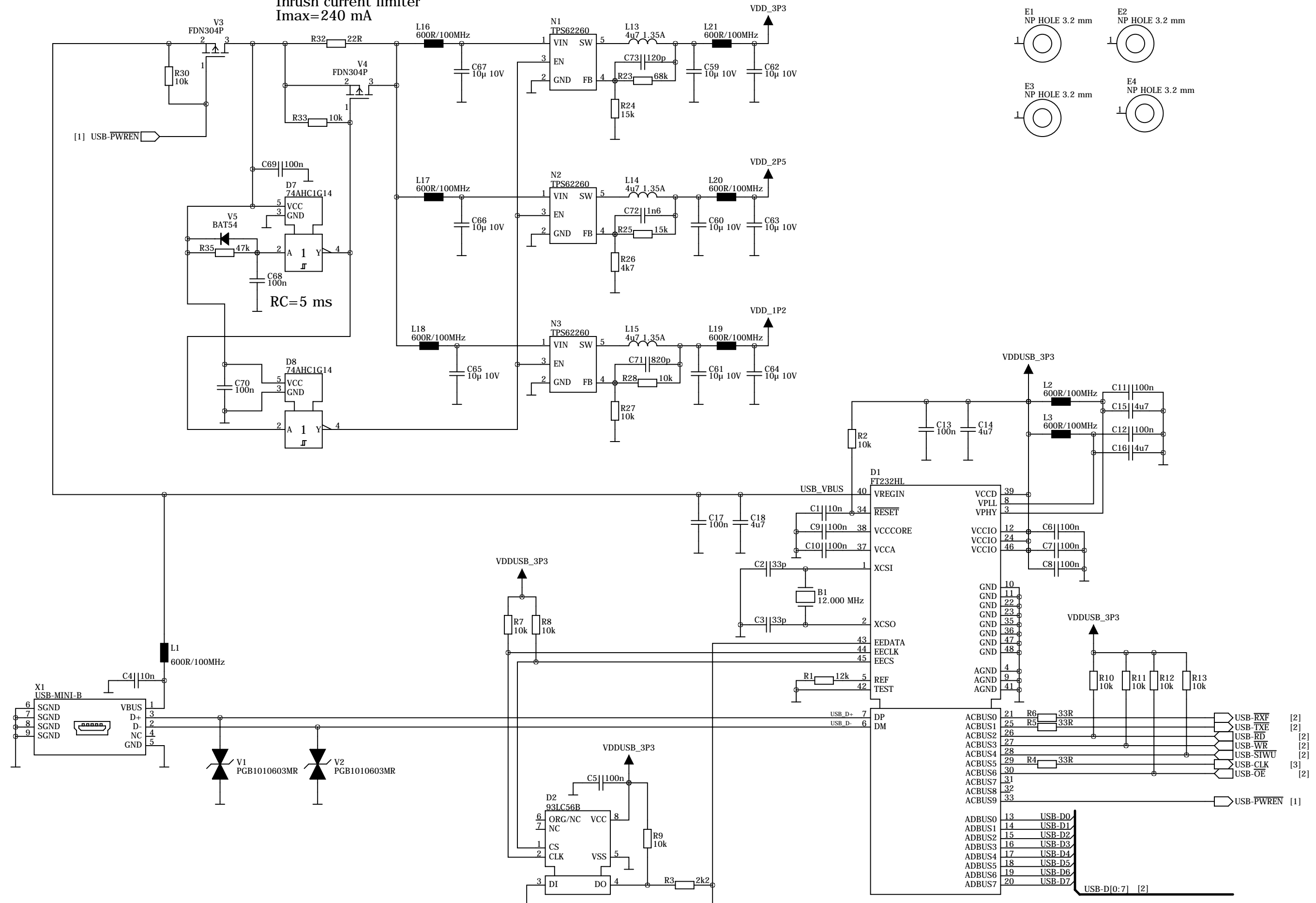
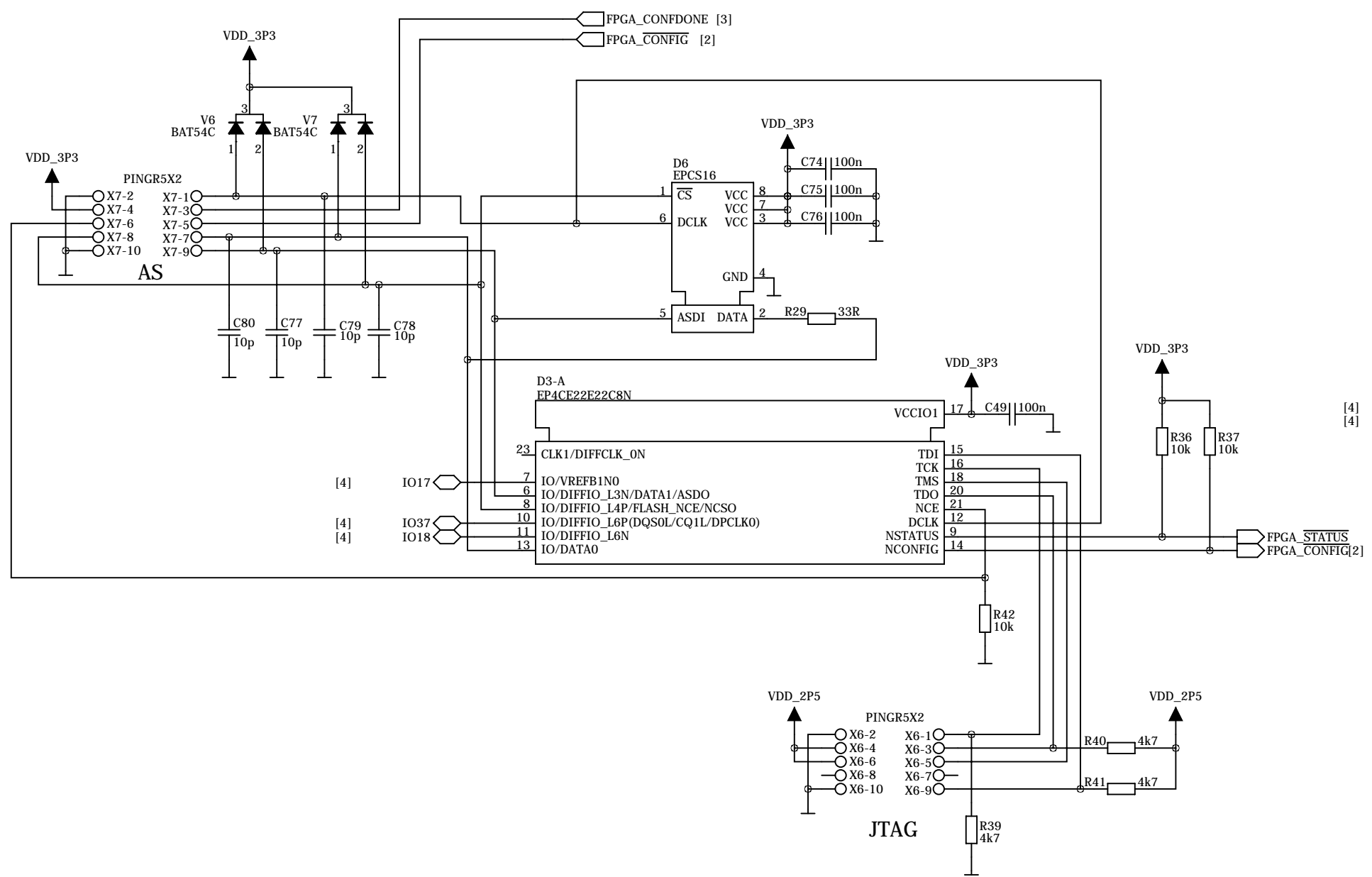
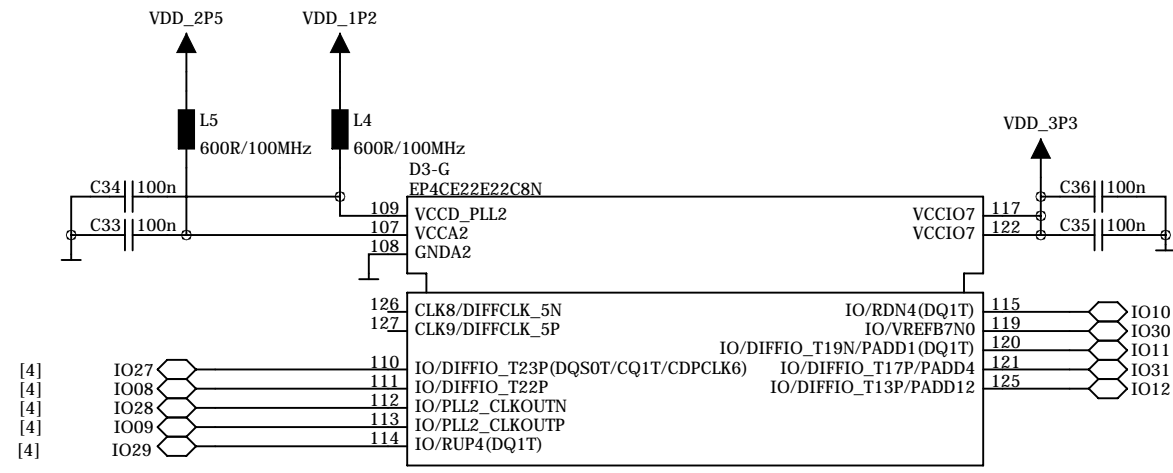


Inrush current limiter
 $I_{max} = 240 \text{ mA}$

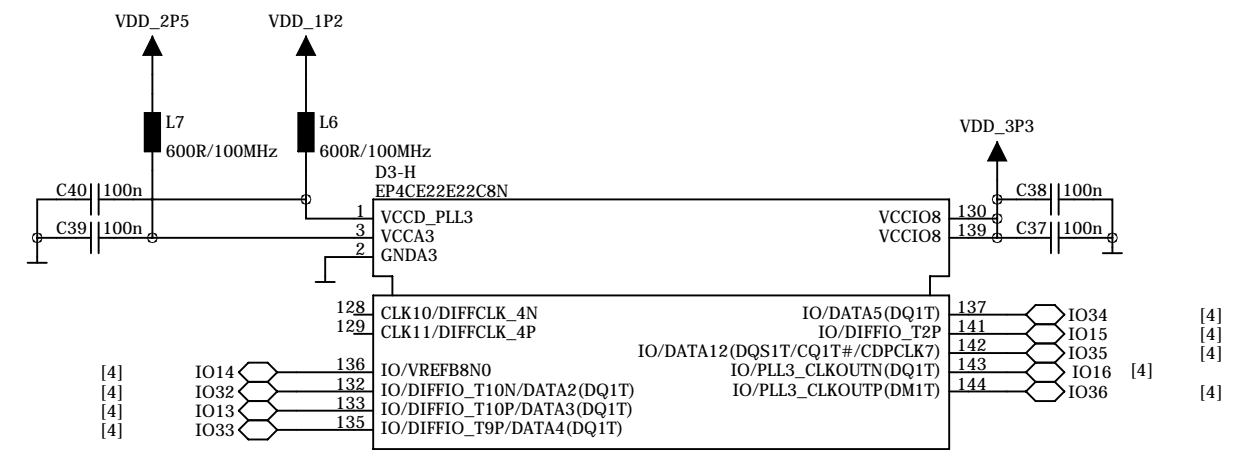


JTA Design	USB-FPGA HSIO		Version 01 Sheet 1 OF 4
	USB		
	Design date	File name	
	2013-01-16	USB-FPGA HSIO 01.sch	

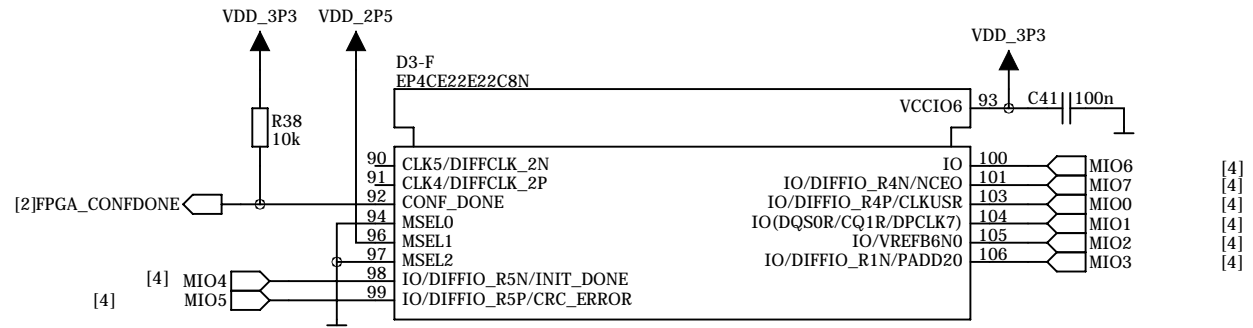




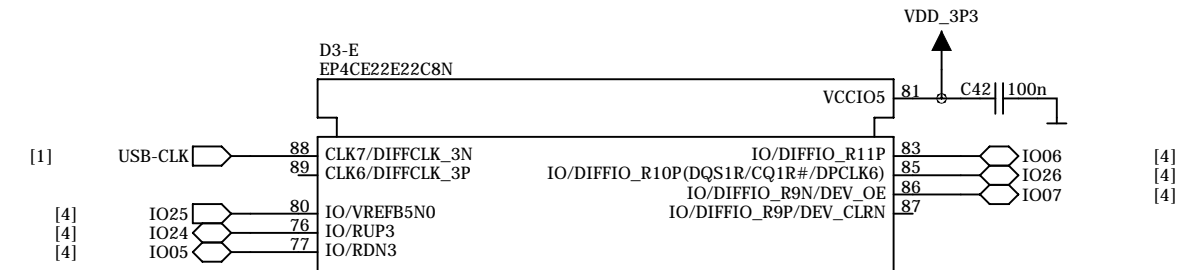
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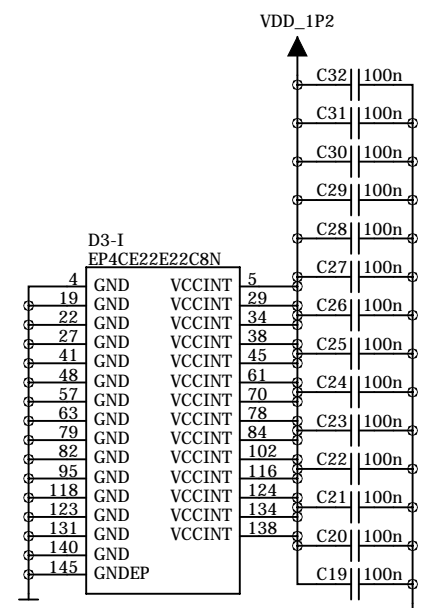


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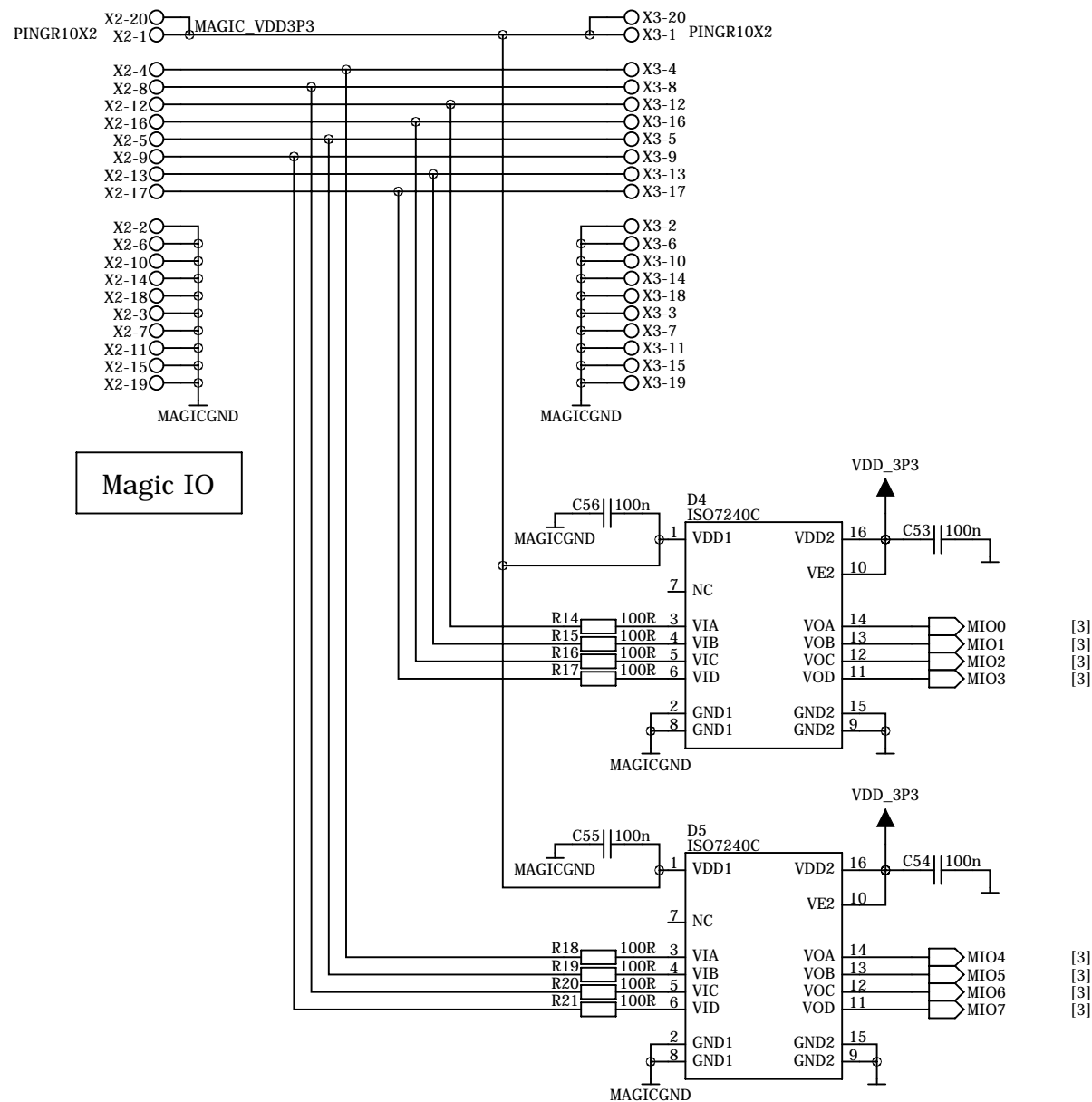


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JTA Design	USB-FPGA HSIO Sheet Description		Version 01
	Design date 2013-01-16	File name USB-FPGA HSIO 01.sch	Sheet 3 OF 4



FPGA pin map			
Signal	FPGA PIN	Signal	FPGA PIN
50 MHz oscillator	24		
USB CLK	88		
USB \overline{RXF}	52		
USB \overline{TXE}	53		
USB \overline{RD}	60		
USB \overline{WR}	64		
USB \overline{SIWU}	59		
USB \overline{OE}	58		
USB D0	39	MIO0 (X2/X3-12)	103
USB D1	43	MIO1 (X2/X3-13)	104
USB D2	44	MIO2 (X2/X3-16)	105
USB D3	46	MIO3 (X2/X3-17)	106
USB D4	49	MIO4 (X2/X3-4)	98
USB D5	50	MIO5 (X2/X3-5)	99
USB D6	51	MIO6 (X2/X3-8)	100
USB D7	42	MIO7 (X2/X3-9)	101
IO01	65	IO21	66
IO02	67	IO22	68
IO03	69	IO23	71
IO04	72	IO24	76
IO05	77	IO25	80
IO06	83	IO26	85
IO07	86	IO27	110
IO08	111	IO28	112
IO09	113	IO29	114
IO10	115	IO30	119
IO11	120	IO31	121
IO12	125	IO32	132
IO13	133	IO33	135
IO14	136	IO34	137
IO15	141	IO35	142
IO16	143	IO36	144
IO17	7	IO37	10
IO18	11	IO38	28
IO19	30	IO39	31
IO20	32	IO40	33

