Freescale Technology Forum

Design Innovation.

June 19, 2008

Signal Integrity, EMI & Crosstalk Control

in High Speed Digital Circuits & PC Boards.

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Agenda - Control of SI & EMI

- Recommended Reading Lists
- Electrical Domain (R, C, L, Currents, Frequency, etc.)
- Er, Propagation Time/Velocity and Rise Distance
- Transmission Lines and How to Resolve Impedance
- Effect of Loading on Transmission Lines
- Trace Routing and Termination Schemes
- Signal & Wave Attenuation
- Connectors and other Discontinuities
- Understanding Cross Talk
- Power Distribution and Decoupling
- EMI - Understanding and Control
- Planes and Plane Splits
- PC Board Stack-ups that work

High Speed Design Reading List

1. Right the First Time- A Practical Handbook on High Speed PCB and System Design - Volumes I & II - Lee W. Ritchey (Speeding Edge) - ISBN 0-9741936-0-7
2. High Speed Digital System Design- A handbook of Interconnect Theory and Practice - Hall, Hall and McCall (Wiley Interscience 2000) - ISBN 0-36090-2
3. High Speed Digital Design- A Handbook of Black Magic - Howard W. Johnson & Martin Graham (Prentice Hall) - ISBN 0-13-395724-1
4. High Speed Signal Propagation- Advanced Black Magic - Howard W. Johnson & Martin Graham - (Prentice Hall) - ISBN 0-13-084408-X
5. Signal Integrity Simplified - Eric Bogatin (Prentice Hall) - ISBN 0-13-066946-6
6. Signal Integrity Issues and Printed Circuit Design - Doug Brooks (Prentice Hall) - ISBN 0-13-141884-X

EMI Reading List

1. PCB Design for Real-World EMI Control - Bruce R. Archambeault (Kluwer Academic Publishers Group) - ISBN 1-4020-7130-2
2. Digital Design for Interference Specifications- A Practical Handbook for EMI Suppression - David L. Terrell & R. Kenneth Keenan (Newnes Publishing) - ISBN 0-7506-7282-X
3. Noise Reduction Techniques in Electronic Systems - Henry Ott (2nd Edition - John Wiley and Sons) - ISBN 0-471-85068-3
4. Introduction to Electromagnetic Compatibility - Clayton R. Paul (John Wiley and Sons) - ISBN 0-471-54927-4
5. EMC for Product Engineers - Tim Williams (Newnes Publishing) - ISBN 0-7506-2466-3
6. Grounding & Shielding Techniques - Ralph Morrison (5th Edition - John Wiley & Sons) - ISBN 0-471-24518-6

Read Books NOT IC App Notes

"Circuit Application notes produced by IC manufacturers should be assumed Wrong until Proven Right!"

Lee W. Ritchey

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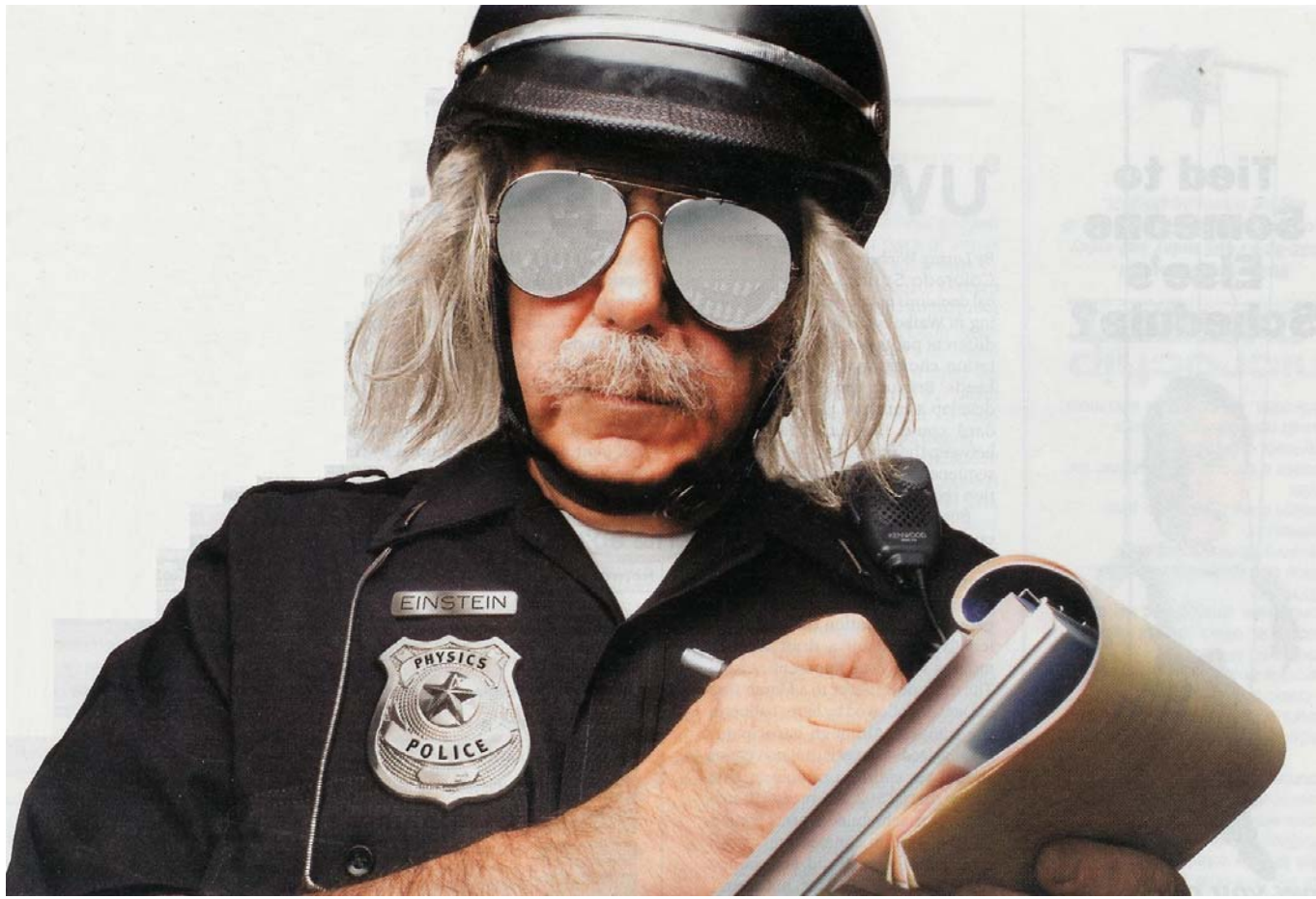
Read Books NOT IC App Notes

What our industry needs!?!?!?



Source:
CoilCraft

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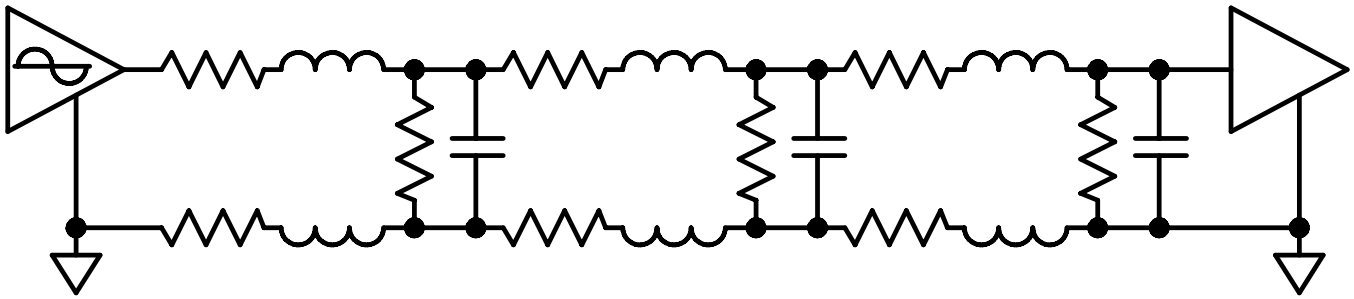
PC Board Properties

- A Transmission Line is any Pair or Wires or Conductors used to Move Energy From point A to point B, Usually of Controlled Size and in a Controlled Dielectric to create a Con-trolled Impedance (Zo).



Evenly Distributed R, L, G & C – $Zo=\sqrt{\frac{R+j\omega L}{G+j\omega C}}$

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PC Board Properties

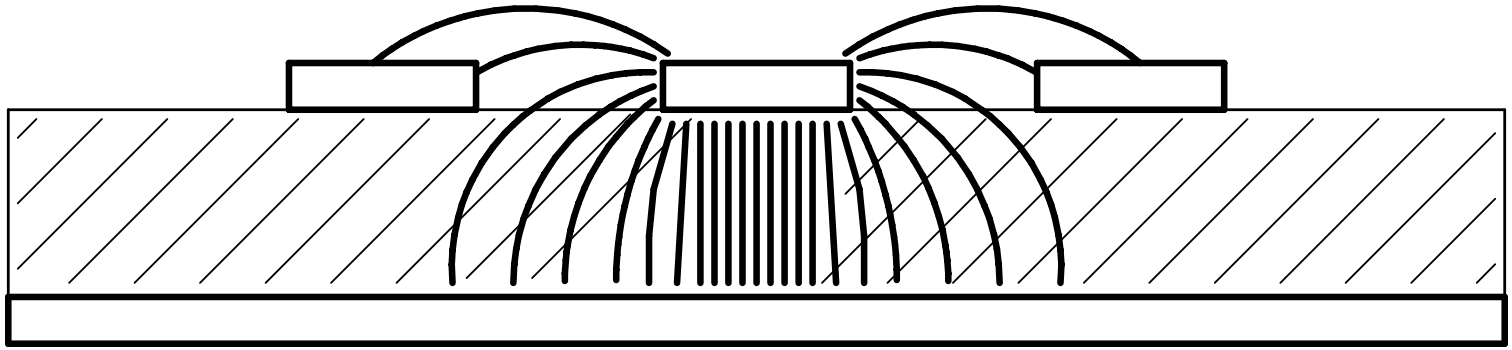
- Below 1 - 2 GHz ‘R’ and ‘G’ are less significant in Digital Circuits and can be ignored.
- Therefore, at lower Frequencies -

$$Zo = \sqrt{\frac{Lo}{Co}}$$

- **Notice That Zo is independent of Length.**

PC Board Properties - Capacitance

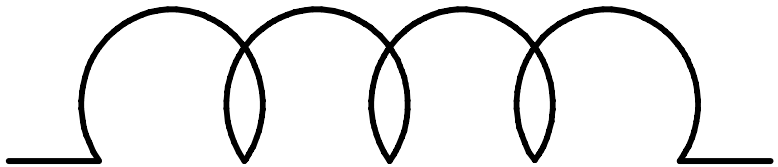
- A PC Board Trace forms a Capacitance with ALL adjacent Conductive Surfaces.



- The Strongest Region is Between the Trace and its Return Path (i.e.- Ground Plane).

(- If we structure the Board Well -)

PC Board Properties - Inductance



- Property of the Circuit Allowing Energy Storage in a Field Induced by Current Flow.
- Field consists of Magnetic Flux Lines which Surround the Conductor.
- Energy causes Inertia to Changes in Current.
- Inertia causes Frequency Dependence.

PC Board Properties - Inductance

In Circuits and PC Boards there are 2 Issues we need to understand regarding Inductance:

First-

- Function of Trace Length and Cross-Sectional Area (Width x Thickness).
- Decreases if Trace is Shorter, Wider, Thicker.
- .020” Wide, 1 oz, 1.0” Long Trace placed very far return path = 25 nH.
- Must be Widened to 1.0” to = 12.5 nH.

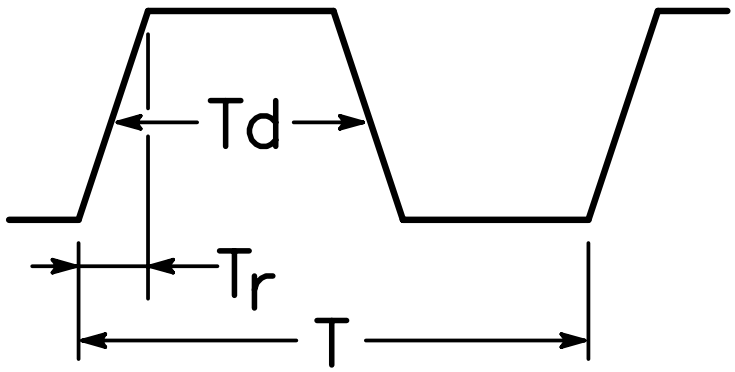
PC Board Properties - Inductance

Second-

- Function of Closed Loop Area between the Trace and its Return Path.
- Inductance Decreases as Closed Loop Area Decreases (Referred to as Self Inductance).
- .020” Wide, 1.0” Long (25nH) Trace placed above its Return Path (next layer plane) w/ .010” separation (trace - plane) = 6.5nH.

Operating Frequency Bandwidth

Time Domain

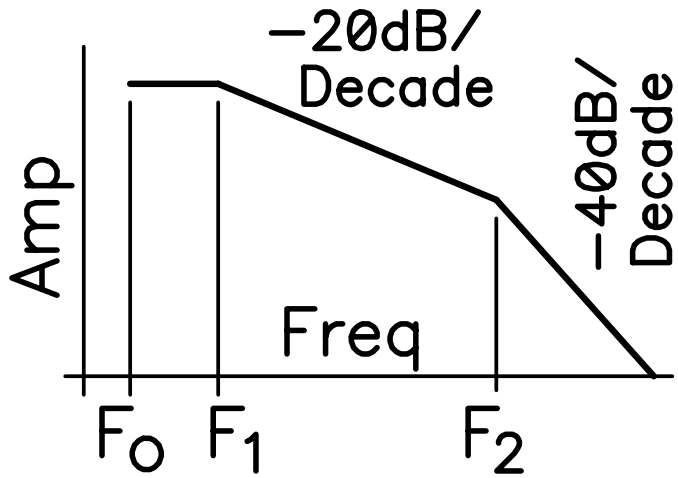


$$F_o = 1/T$$

$$F_1 = 1/(\pi Td)$$

$$F_2 = 1/(\pi Tr)$$

Frequency Domain



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Operating Frequency Bandwidth

- Highest Frequency of concern IS NOT the Clock.
- Is Frequency of the High Harmonics necessary to create the Fast Rising Edges of the Signal.
- Called Maximum Pulse Frequency.

F (Freq-GHz) = .50 / Tr (rise/fall time-ns *)

* (Tr = 10-90% (Typical))

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- Frequency Bandwidth is from Clock to Maximum Pulse Frequency.

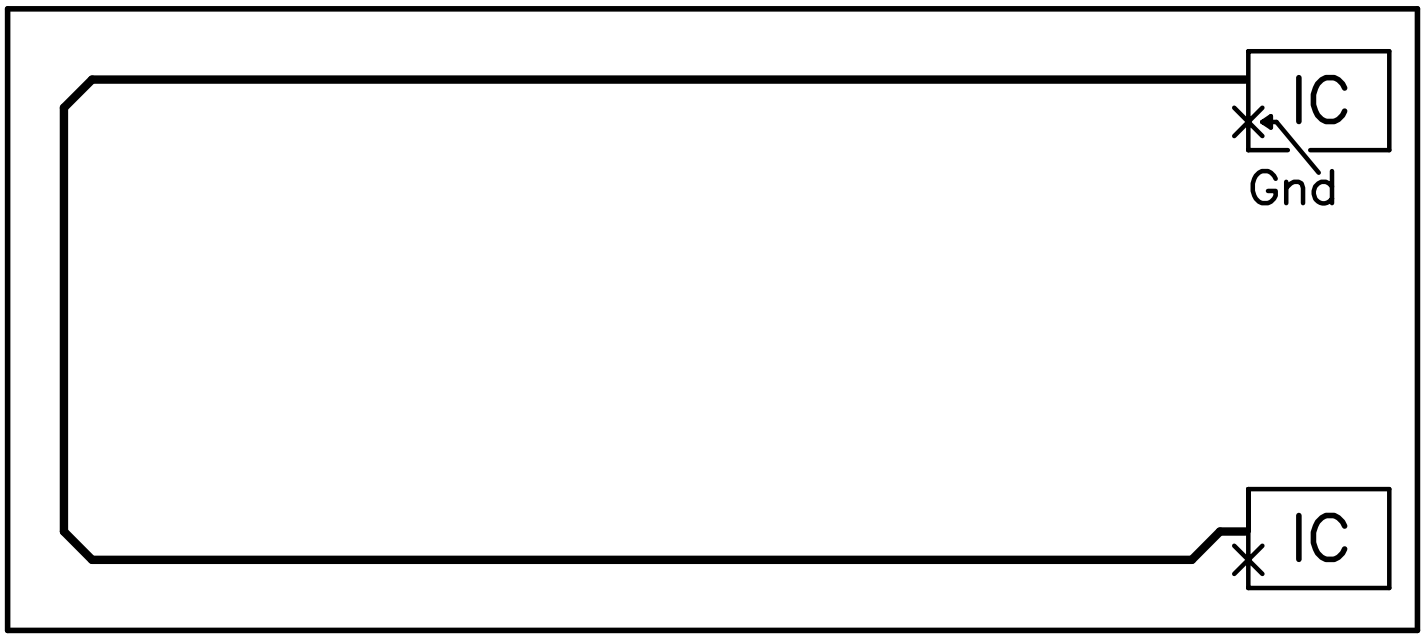
Current Paths

- Driven Signal MUST return to its Source.
- Signal Path is defined by PCB Trace.
- DC Signal Return -
  - Path of Least Resistance.
- High Frequency Signal Return -
  - Path of Least Impedance.
- High Frequency Trace Routed over a Plane-
  - Return Current Flows Directly under Signal.

- 2 Layer Microwave Style PC Board -

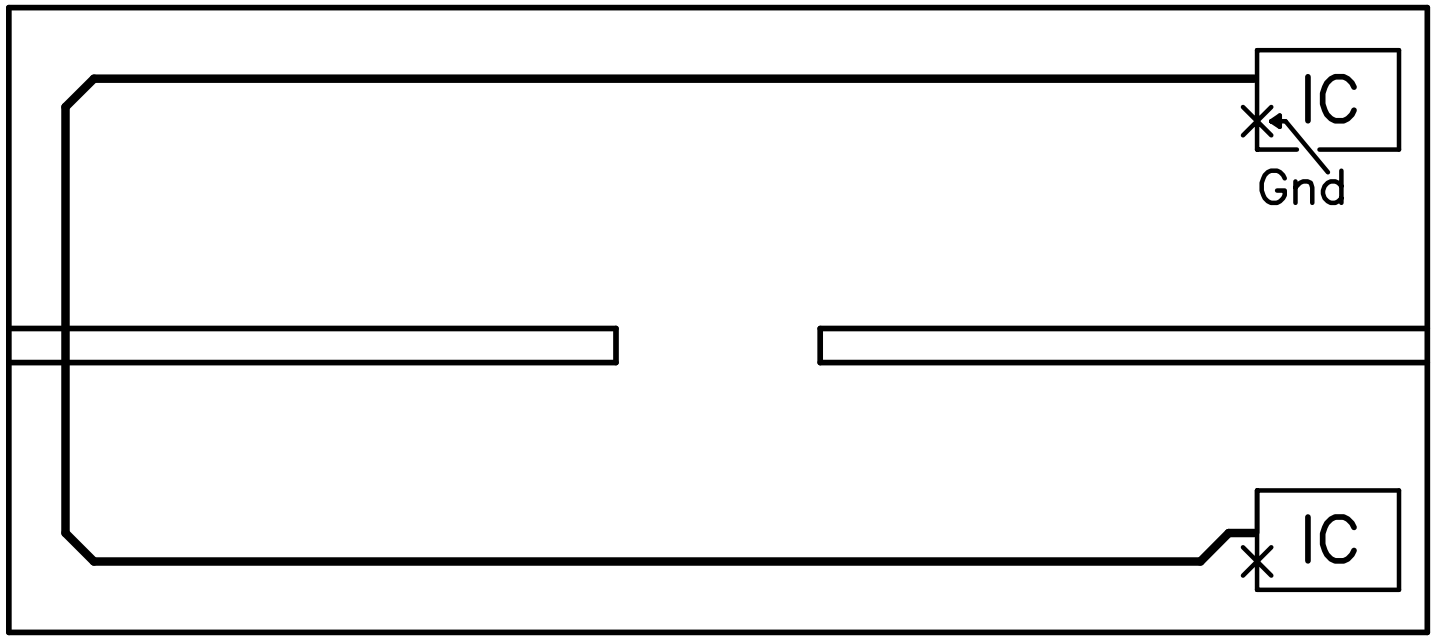
L1- Routed Signal, routed Power and poured Ground copper.

L2- Ground.



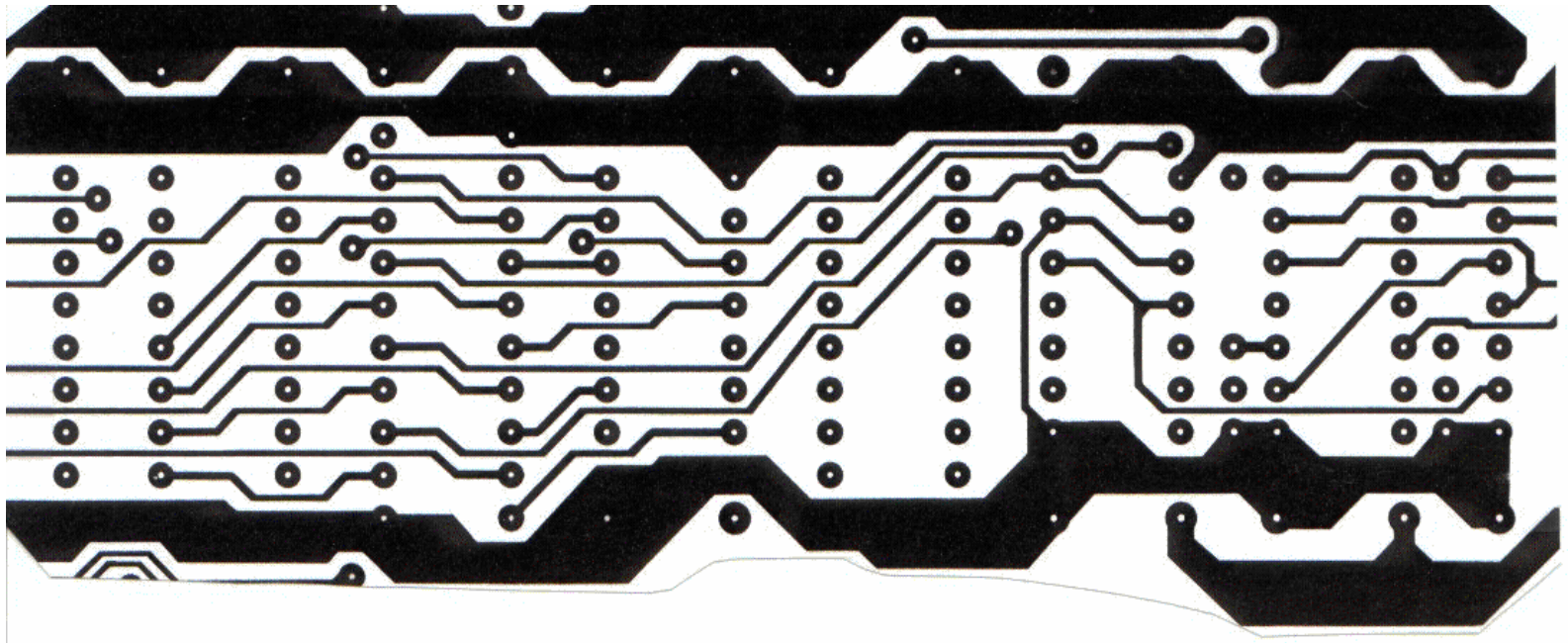
Where does signal's return current flow?

- What happens if Return Plane is Split???
  - Now where does return current flow?



What if the Plane is not ‘Ground’??????

- What if NO Plane exists in the board??????

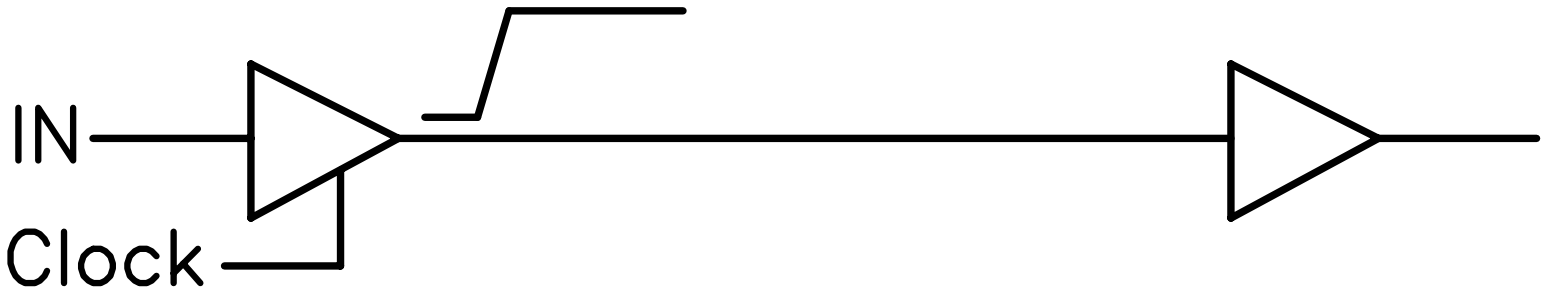


- Now where does Return Current flow???

(Usually Acceptable if all lines are Lumped)

Transmission Line Characteristics

- When do Problems begin???
  - When the Time to Propagate a Conductor's Length is Greater than 1/4 of the Signal Rise or Fall Time.



- Most extreme when Time to Propagate the Conductor's Length is Equal to or Greater than the Signal Rise or Fall Time.

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Reflections -

- When a Pulse propagates a Long Transmission Line of Impedance Zo and reaches a Load of the same Impedance, ALL the energy is Transferred.

- If the 'Down Stream' Impedance (Zload) is different than that of the Line (Zo), then a percentage of the Pulse is Reflected back toward the Source.

$$\% \text{ Reflection} = \frac{Zload - Zo}{Zload + Zo} X\ 100$$

Relative Permittivity -

- Measure of the affect a material has on the Capacitance of a Pair of Conductors compared to the same Pair in a Vacuum
- Also, affects travel time (Propagation Time) of a signal in that Pair of Conductors.
- Relative Permittivity is expressed using Greek letter "Epsilon", followed by lower case "r".

(i.e.- ε_r or Er (aka DK (Dielectric Constant.))

Transmission Line Characteristics

Relative Permittivity -

Er (ε_r) of FR4 -

- Frequency Dependent.
- Dependent on Glass-to-Resin Ratio.
- Materials available w/ More Constant Er-
  - Most Materials designed for High Speed.
  - All PTFE based Materials.

FR-4 Copper Clad Laminate Construction Selection Guide

REG#	THICKNESS	CONSTRUCTION	% RC	DK	DK. TOL.	DS	Z CTE	THICK TOL	CHEM	MEASLE	AVAIL	COST	FLAT	SMOOTH	DRILL
FR-4 00	0.05mm	106	70	4.08	○	○	○	○	●	●	○	○		+	+
FR-4 01	0.07mm	1080	60	4.25	◒	●	○	○	●	●	○	●		+	+
FR-4 02	0.08mm	2x106	64	4.15	●	○	○	●	◒	●	○	○		+	+
FR-4 03	0.11mm	2x106	72	4.10	◒	●	○	◒	○	●	○	○		+	+
FR-4 04	0.11mm	2113	57	4.30	●	○	◒	●	○	○	○	●			+
FR-4 05	0.14mm	106/2113	56	4.30	●	●	◒	●	◒	○	●	○	–	+	+
FR-4 06	0.13mm	2x1080	59	4.25	○	⊗	◒	○	●	◒	◒	◒		+	+
FR-4 07	0.13mm	2116	53	4.40	○	○	●	○	○	○	○	●			
FR-4 08	0.16mm	106/2116	51	4.45	●	●	○	●	○	○	●	○	–		
FR-4 09	0.16mm	1080/2113	54	4.40	●	○	○	●	○	○	◒	○	–		–
FR-4 10	0.18mm	2x2113	50	4.50	○	○	○	◒	◒	○	○	○			+
FR-4 11	0.18mm	7628	40	4.75	○	○	●	◒	⊗	⊗	○	●		–	–
FR-4 12	0.21mm	2113/2116	50	4.50	●	●	○	●	○	○	●	○	–		
FR-4 13	0.21mm	2x2116	47	4.55	●	○	○	●	○	○	●	○	+		
FR-4 14	0.25mm	2x2116	52	4.4	◒	○	◒	◒	◒	◒	●	◒	+		–
FR-4 15	0.26mm	7628/1080	47	4.6	●	●	●	●	◒	○	◒	●	–	–	
FR-4 16	0.26mm	2x1080/2116	55	4.6	●	○	○	●	●	●	○	◒	+	+	
FR-4 17	0.31mm	2x1080/7628	47	4.6	●	●	◒	●	●	●	●	○	+	+	–
FR-4 18	0.32mm	7628/2116	47	4.6	●	◒	●	●	○	○	○	●	–	–	–
FR-4 19	0.37mm	2x7628	41	4.7	●	●	●	●	◒	○	●	●	+	–	–
FR-4 20	0.37mm	2x2113/7628	46	4.8	◒	●	◒	●	◒	●	◒	○	+		–
FR-4 21	0.43mm	2x2116/7628	48	4.5	●	●	◒	●	◒	◒	○	○			–
FR-4 22	0.43mm	2x7628/1080	43	4.7	●	●	●	●	◒	○	●	●	+	–	–
FR-4 23	0.48mm	2x7628/2116	43	4.8	●	●	◒	●	○	○	●	◒	+	–	–
FR-4 24	0.51mm	2x1080/2x7628	46	4.5	●	●	◒	●	●	●	○	○	+	+	–
FR-4 25	0.53mm	3x7628	40	4.7	●	●	●	●	○	◒	●	●	+	–	–
FR-4 26	0.64mm	2x2116/2x7628	47	4.6	●	●	◒	●	◒	●	●	●	+		–
FR-4 27	0.61mm	3x7628/1080	42	4.7	●	●	●	●	◒	○	●	●	–	–	–
FR-4 28	0.74mm	4x7628	41	4.7	●	●	●	●	○	○	●	●	+	–	–
FR-4 29	0.74mm	2x2113/3x7628	44	4.7	●	●	○	●	◒	◒	○	○	+		–
FR-4 30	0.75mm	4x7628/1080	42	4.7	●	●	◒	●	○	◒	◒	◒	+	–	–
FR-4 31	1.52mm	8x7628	42	4.7	●	●	◒	◒	○	○	●	◒	+	–	–

● Better + ◒ ○ Blank ◒ ⊗ Worse

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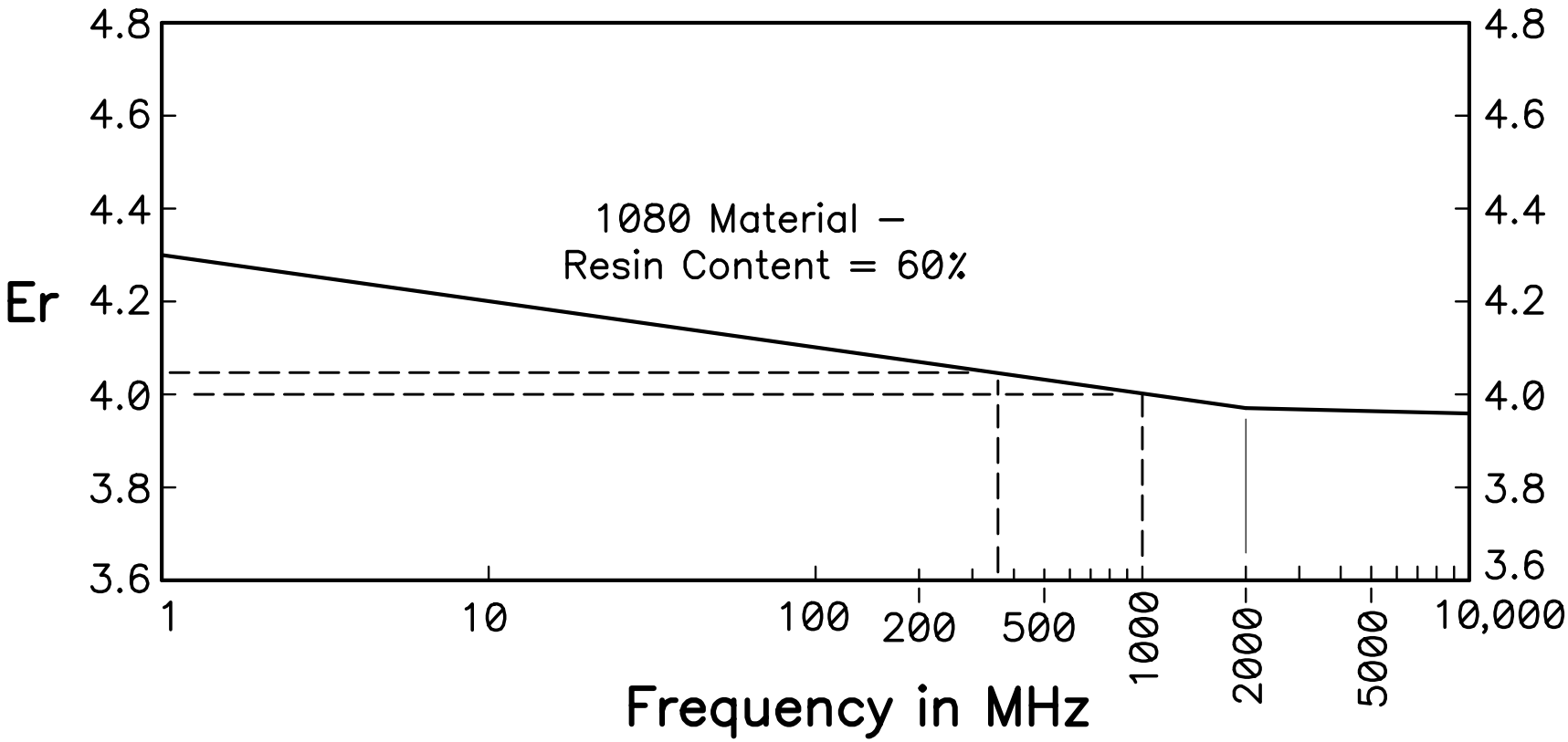
- Er of FR4 vs Frequency -



Also see Nelco and Isola Websites.

- Standard Board Stack vs Zo -

Layers	Thickness	Cross Section Diagram	Layer Definition	Cu. & Diel. Tol.
	0.7	mmmmmmmmmmm		*Mask*
	1.4	x y y y y y y y y y y y z		*Plating*
L01	0.7	l c r	Signal	H oz.
	7.5	1 x 7628HR		(+\- 1.0)
L02	1.4	l ccccccccccccccccc r	Plane	1 oz.
	38.0	0.038 1/1		(+\- 1.0)
L03	1.4	L CCCCCCCCCCCCCCCCC R	Plane	1 oz.
	7.5	1 x 7628HR		(+\- 1.0)
L04	0.7	L C R	Signal	H oz.
	1.4	X Y Y Y Y Y Y Y Y Y Y Y Z		*Plating*
	0.7	mmmmmmmmmmm		*Mask*

Total: **61.4** **Est. Finish Thickness Over Mask**

6 mil line (Outer Layer - 500 MHz) = 63Ω

5 mil line (Inner Layer - 500 MHz) = 61Ω

- Standard Board Stack vs Zo -

Layers	Thickness	Cross Section Diagram	Layer Definition	Cu. & Diel. Tol.
	0.7	mmmmmmmmmmm		*Mask*
	1.4	x y y y y y y y y y y y z		*Plating*
L01	0.7	l c r	Signal	H oz.
	7.5	**1 x 7628HR**		(+\- 1.0)
L02	1.4	l ccccccccccccccccc r	Plane	1 oz.
	14.0	**0.014 1/1**		(+\- 1.0)
L03	1.4	L C R	Signal	1 oz.
	7.0	**1 x 7628HR**		(+\- 1.0)
L04	1.4	l c r	Signal	1 oz.
	14.0	**0.014 1/1**		(+\- 1.0)
L05	1.4	L CCCCCCCCCCCCCCCCC R	Plane	1 oz.
	7.5	**1 x 7628HR**		(+\- 1.0)
L06	0.7	L C R	Signal	H oz.
	1.4	X Y Y Y Y Y Y Y Y Y Y Y Z		*Plating*
	0.7	mmmmmmmmmmm		*Mask*

Total: **61.2** **Est. Finish Thickness Over Mask**

6 mil line (Outer Layer - 500 MHz) = 63Ω

5 mil line (Inner Layer - 500 MHz) = 56Ω

Propagation Time & Velocity -

- Prop Time is a measure of Signal Travel Time per Unit of Length (i.e.- .17ns per inch).
- Prop Velocity is a measure of Signal Travel Length per Unit of Time (i.e.- 5.89” per ns).
- Prop Time & Velocity (‘Inner Layer’ Signal) -

$$Tpd = \frac{\sqrt{Er}}{C} \qquad Vp = \frac{C}{\sqrt{Er}}$$

(Where: c = Speed of Light)

Propagation Time & Velocity -

Effective Relative Er - Microstrip

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1+\frac{12h}{w}}} + 0.04\left(1-\frac{w}{h}\right)^2\right] \quad \text{If-} \quad \frac{w}{h} < 1$$

otherwise

$$\varepsilon_{eff} = \left[\frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1+\frac{12h}{w}}}\right]\right]$$

For Propagation of Outer layer Traces - Plug Eeff into Equations on previous page -OR-

Propagation Time & Velocity -

- The Outer Layer (Microstrip) Equivalent -

$$Tpd = \frac{\sqrt{.457Er + .67}}{C}$$

$$Vp = \frac{C}{\sqrt{.457Er + .67}}$$

(Where: c = Speed of Light)

Rise Distance / Max Line Length -

- The Distance a Pulse can Travel in the Time it takes to Rise (Sr) can be calculated by adding Rise Time to the Prop Velocity equation:

Inner Layer- $$Sr = \frac{Tr \times C}{\sqrt{Er}}$$

Outer Layer- $$Sr = \frac{Tr \times C}{\sqrt{.457Er + .67}}$$

= Max Uncontrolled Line is 1/4 Rise Distance =

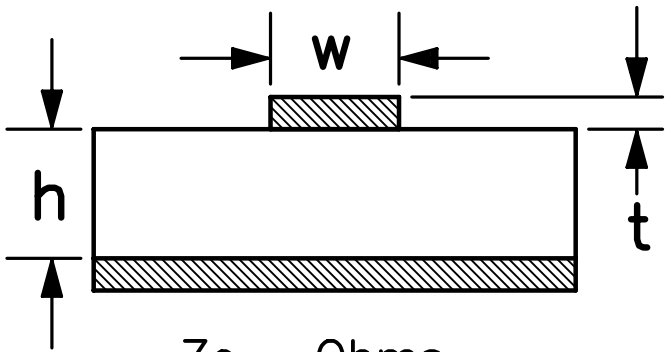
Logic Families / Rise Time / Max Line Length -

DEVICE TYPE	RISETIME	Max Line Length-Inner (Inch/mm)	Max Line Length-Outer (Inch/mm)
Standard TTL	5.0 nSec	7.27 / 185	9.23 / 235
Schottky TTL	3.0 nSec	4.36 / 111	5.54 / 141
10K ECL	2.5 nSec	3.63 / 92	4.62 / 117
ASTTL	1.9 nSec	2.76 / 70	3.51 / 89
FTTL	1.2 nSec	1.75 / 44	2.22 / 56
BICMOS	0.7 nSec	1.02 / 26	1.29 / 33
10KH ECL	0.7 nSec	1.02 / 26	1.29 / 33
100K ECL	0.5 nSec	.730 / 18	.923 / 23
GaAs	0.3 nSec	.440 / 11	.554 / 14

(Calculated assuming a nominal Er = 4.1)

Transmission Line Impedance Calculations

- Microstrip -



Zo = Ohms

Co = nF/inch

$$Zo = \frac{87}{\sqrt{Er + 1.41}} \times \ln\left(\frac{5.98h}{0.8w + t}\right)$$

$$Co = \frac{Tpd\ (ns/inch)}{Zo\ (Ohms)}$$

Assumes LPI Soldermask over Bare Copper.

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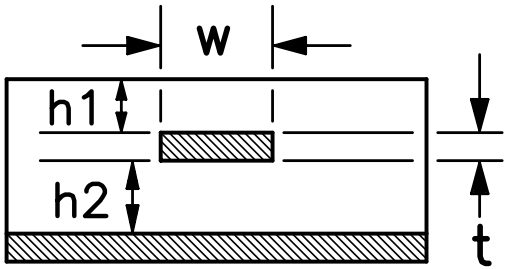
Transmission Line Impedance Calculations

- Embedded Microstrip -



Zo = Ohms
Co = nF/inch

$$Zo = \frac{87}{\sqrt{Er + 1.41}} \times \ln\left(\frac{5.98h2}{0.8w + t}\right) \times \left(1 - \frac{h1}{0.1}\right)$$

$$Co = \frac{Tpd\ (ns/inch)}{Zo\ (Ohms)}$$

Dimensions Must be in Inches-
i.e.- 8 mils must be expressed as .008".

To use other units, convert 0.1
to 100 for mils
to 2.54 for mm
to .254 for cm

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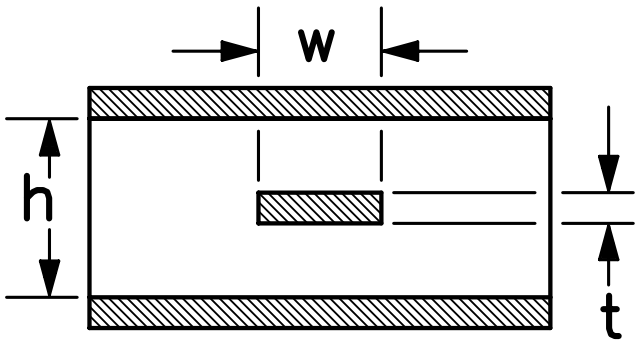
Transmission Line Impedance Calculations

- Centered Stripline -



Zo = Ohms

Co = nF/inch

$$Zo = \frac{60}{\sqrt{Er}} \times \ln\left(\frac{4 \times h}{0.67\pi(0.8w + t)}\right)$$

$$Co = \frac{Tpd\ (ns/inch)}{Zo\ (Ohms)}$$

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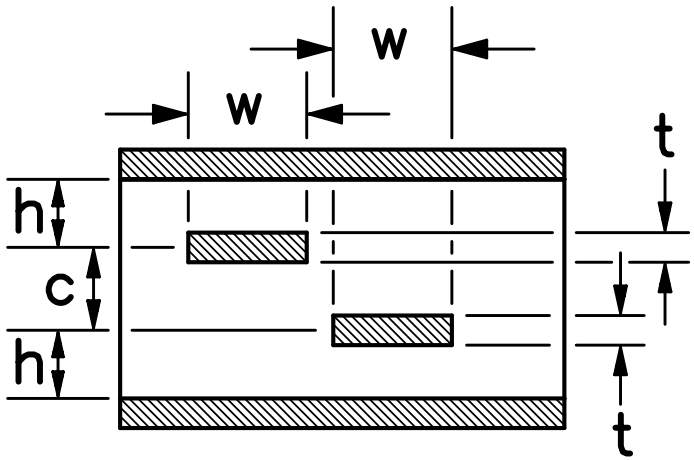
Transmission Line Impedance Calculations

- Dual / Offset Stripline -



Zo = Ohms

Co = nF/inch

$$A = \frac{60}{\sqrt{Er}} \times \ln\left(\frac{8 \times h}{0.67\pi(0.8w + t)}\right)$$

$$B = \frac{60}{\sqrt{Er}} \times \ln\left(\frac{8\,(h + c)}{0.67\pi(0.8w + t)}\right)$$

$$Zo = \frac{A + B}{2}$$

$$Co = \frac{Tpd\ (ns/inch)}{Zo\ (Ohms)}$$

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Transmission Line Impedance Calculations

- Equations to Use-
  - Those Presented (Derived by Fabricators).
  - Others provided by YOUR Fabricator(s).
  - Multiple Term RF/Microwave Equations.
- Zo Calculator(s).
  - Some are Costly.
  - Some are Free.
  - Some are accurate, MOST are NOT.
- 2D Field Solver (Good for Digital Ckts).
- 3D Field Solver (RF/Microwave Ckts).

Transmission Line Impedance Calculations

- Equations presented have Limitations -
  - Best for .004” to .015” Trace Width.
  - Best with Dielectrics of .004” to .020”.
- Most Accurate Range - 35 to 90 Ohms.
- Typical Capacitance - 3pF/inch (50 Ohms).
- Typical Inductance - 8nH/inch (50 Ohms).
- Use hand held Calculator or Spread Sheet.

Transmission Line Impedance Calculations

Good Impedance Calculators -

- Polar Instruments Ltd. (All Basic + Diff).
  - CITS25 (No Longer Sold).
- Tools from UltraCAD (Doug Brooks).
  - www.ultracad.com
- University of Missouri at Rolla
  - Equations from IPC-2251 (Limits similar to equations frpm fab houses) (DON”T use tools based on IPC-D-315, 275, 2221, etc).

Transmission Line Impedance Calculations

Good Impedance Calculators -

- Idea Consulting (Stripline & Diff Stripline)
  - http://www.ideaconsulting.com/index.htm (RF/Microwave based equations)
- Rogers Materials (Basic + Diff Pairs).
  - http://www.rogers-corp.com/mwu/mwi_java/mwij_vp.html (RF/Microwave based equations)

Transmission Line Impedance Calculations

Field Solvers -

- Polar Instruments Ltd. (3D Solver)
  - http://www.polarinstruments.com/
- HyperLynx (Mentor Graphics Inc.) (3D Solver)
  - http://www.hyperlynx.com/
- Ansoft Corp. (3D Field Solver)
  - http://www.ansoft.com/products/si/designersi/
- IPC Resource Website (List of Zo Tools)
  - http://www.ipc.org/contentpage.aspx?pageid=4.5.8

Influence of Nearby Traces -

- Impedance (Zo) Equations assume NO nearby Traces.
- Adjacent Traces routed in Parallel for Longer than Signal Critical Length cause Co-Planar Coupling of Signal.
- Odd Mode Co-Planar Coupling Lowers Impedance.
- Even Mode Co-Planar Coupling Raises Impedance.
- Worse in Microstrip than Stripline.

Microstrip

(3H means Trace Spacing, Edge-to-Edge = 3X Height above Plane)

56 ohm ☞ 58 ohm @ 3H (Even Mode)
56 ohm ☞ 54 ohm @ 3H (Odd Mode)
56 ohm ☞ 59 ohm @ 2H (Even Mode)
56 ohm ☞ 53 ohm @ 2H (Odd Mode)
56 ohm ☞ 62.5 ohm @ 1H (Even Mode)
56 ohm ☞ 49.5 ohm @ 1H (Odd Mode)

Stripline

(3H means Trace Spacing, Edge-to-Edge = 3X Height above Plane)

50 ohm ☞ 50 ohm @ 2H (Even Mode)
50 ohm ☞ 50 ohm @ 2H (Odd Mode)
50 ohm ☞ 51 ohm @ 1H (Even Mode)
50 ohm ☞ 49 ohm @ 1H (Odd Mode)
50 ohm ☞ 53.5 ohm @ 1/2H (Even Mode)
50 ohm ☞ 46.5 ohm @ 1/2H (Odd Mode)

Loaded Circuit Propagation Delay -

- Original Equations are for Static Condition.
- Line Delay Increases due to Load Capacitance.
- Delay in Unterminated or Parallel Term Line:
  Tpd' = Tpd x sqrt{1 + (Cloads / Co (trace))}
- Series Terminated Line has Additional Delay -
  Tpd' = Tpd x [2 (sqrt{1 + (Cloads / Co)} -1) +1]
- Propagation Velocity (Vp') is Inverse of Tp'.
- Remember - Co is a 'per inch' measurement.

Loaded Circuit Trace Impedance -

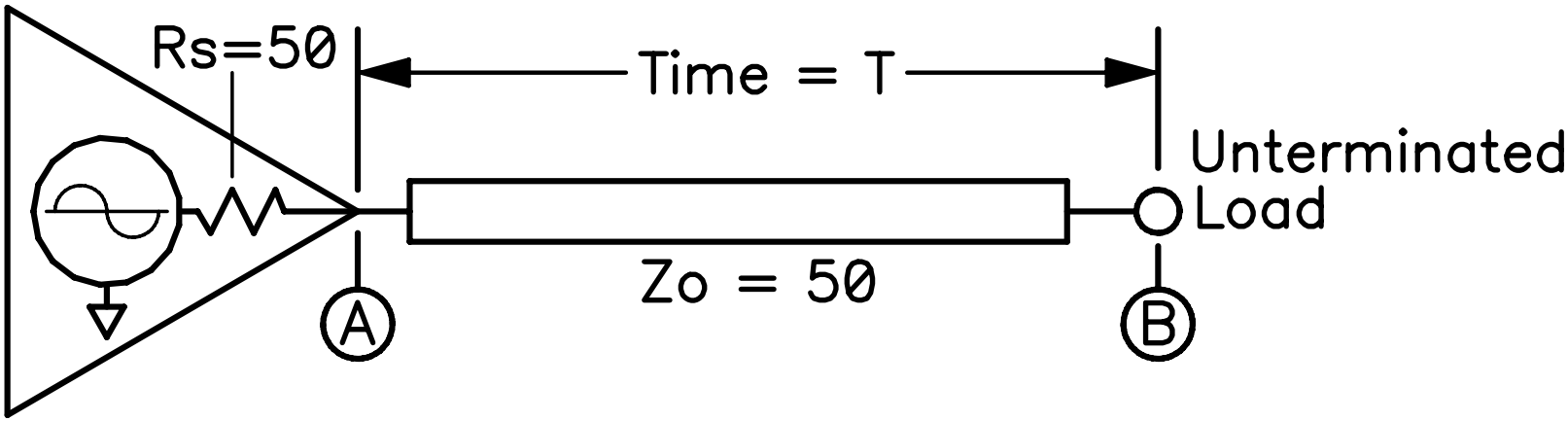
- Original Equations are for Static Condition.
- Impedance decreases due to Load Capacitance.

  Zo(loaded) = sqrt{ Lo / (Co + Cloads) }

  where: Lo = Zo^2 x Co
- Remember - Lo and Co are ‘per inch’, etc measure.

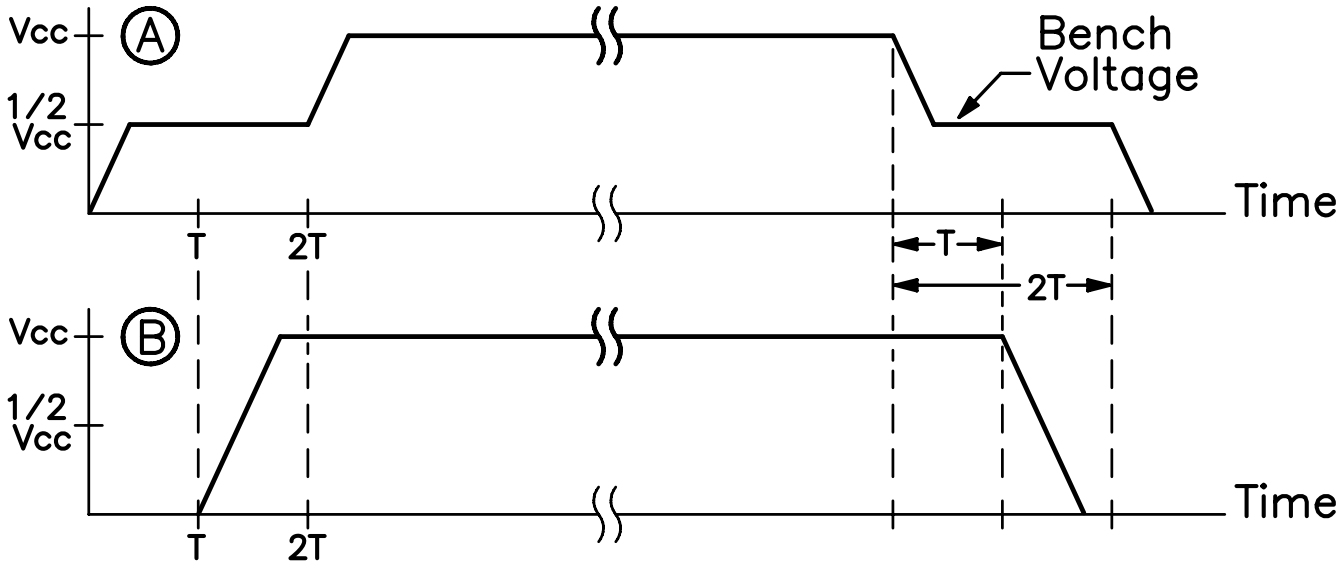
- **If Device Drives Multiple Lines, each Line Must be considered separately.**

Reflection Mode Switching -



- Device with Output Impedance (Rs) equal to Zo sets up a Voltage Divider Between Rs and Zo.
- Divider causes the Initial Line Voltage (Bench Voltage) to be approximately 1/2 Vcc.

Reflection Mode Switching -



- With One Load, Reflection Mode Switching is NOT a Problem.
- Multiple Loads along the Line won't Switch until Reflected Wave raises the Line Voltage.

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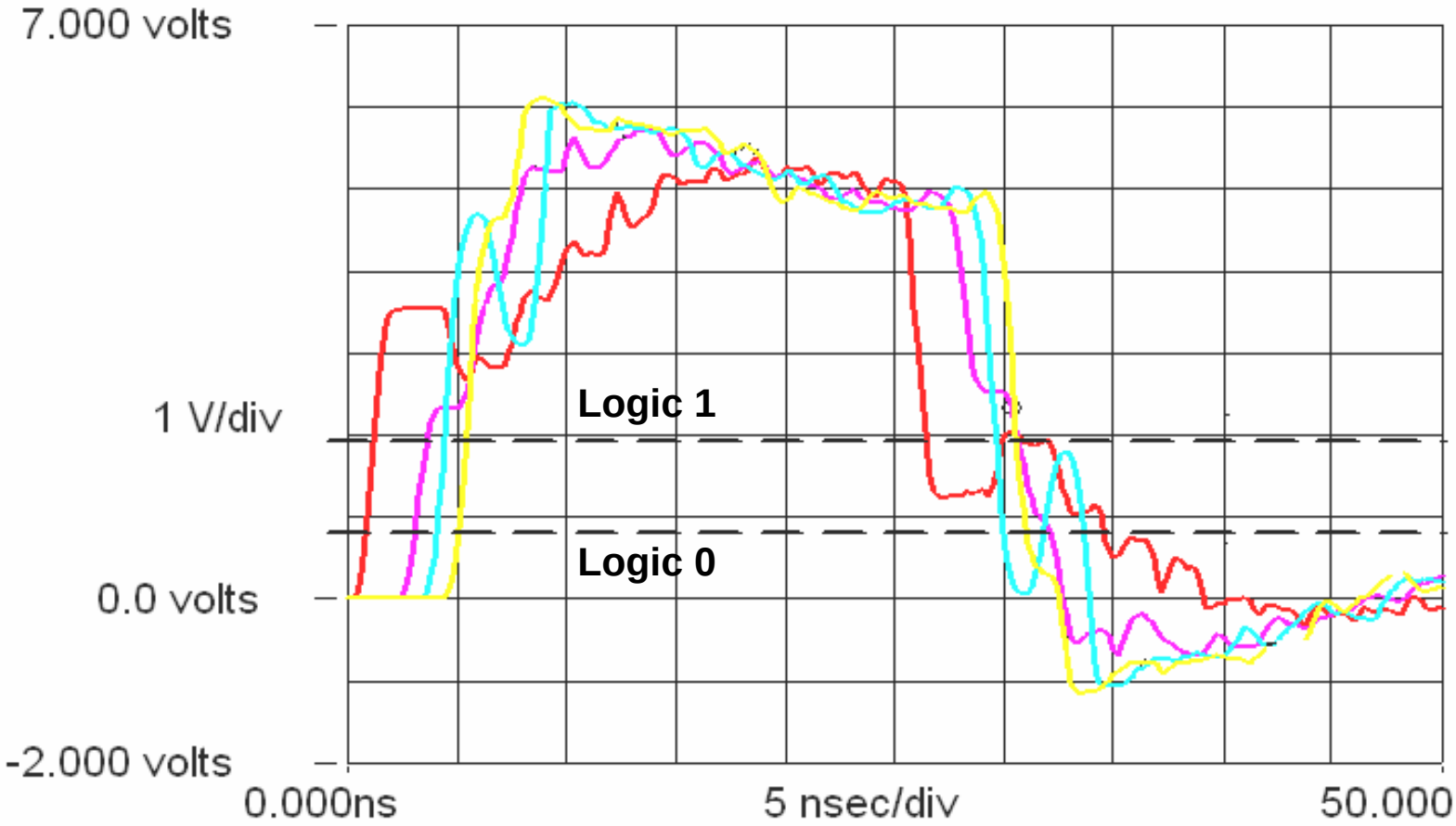
Incident Wave Switching -

- Required with High Clock Rates & Tight Timing.
- Requires Low Output Impedance, High Power Driver.
- Low Power Drivers (High Output Impedance) May Not work.
  - Lumping ALL Loads at end of Line will enable Low Power Driver to work.

Trace Routing and Termination Style



Result of Long Stubs and No Line Termination.

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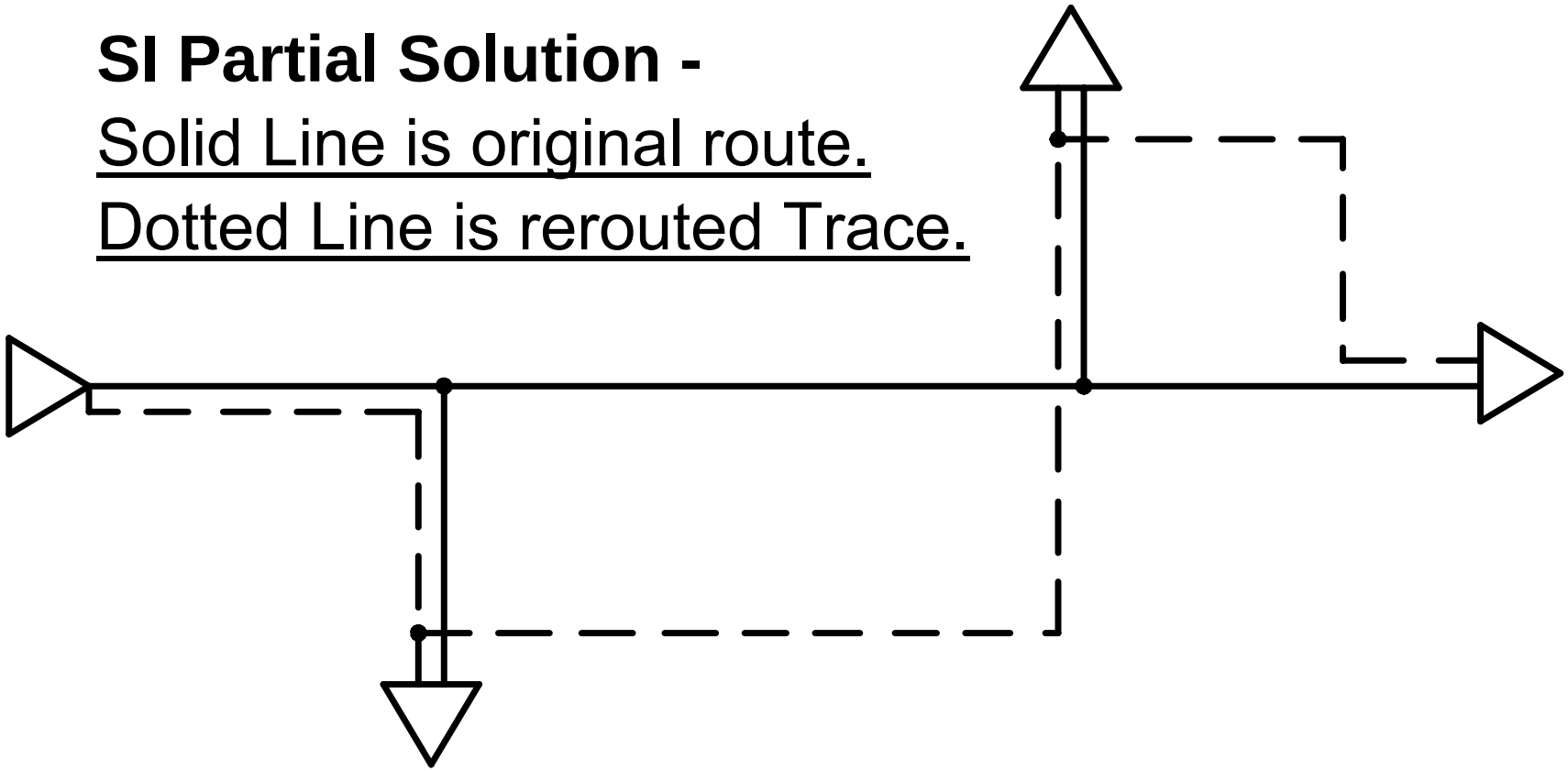
Trace Routing and Termination Style

SI Partial Solution -

Solid Line is original route.

Dotted Line is rerouted Trace.



Keep Stubs Shorter than 1/8 Rise Distance.

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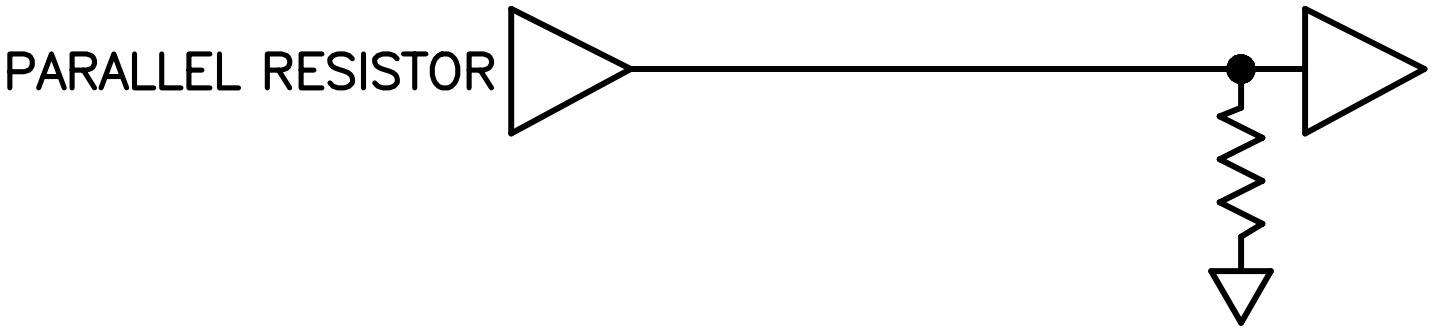
Transmission Line Termination



- Used with Strong Drivers (Needing Incident Wave Switching).
- Some Logic Families Must be Parallel Term (ECL, GTL, etc.).
- Place Resistor within 1/8 Rise Distance of Last Load or just beyond Last Load.
- Resistor Value = Zo.
- Resistor Needed at Both Ends of Bidirectional Net.
- High Power Consumption (DC Load when Output is High).
- Low Power Outputs CANNOT drive this Low Impedance.

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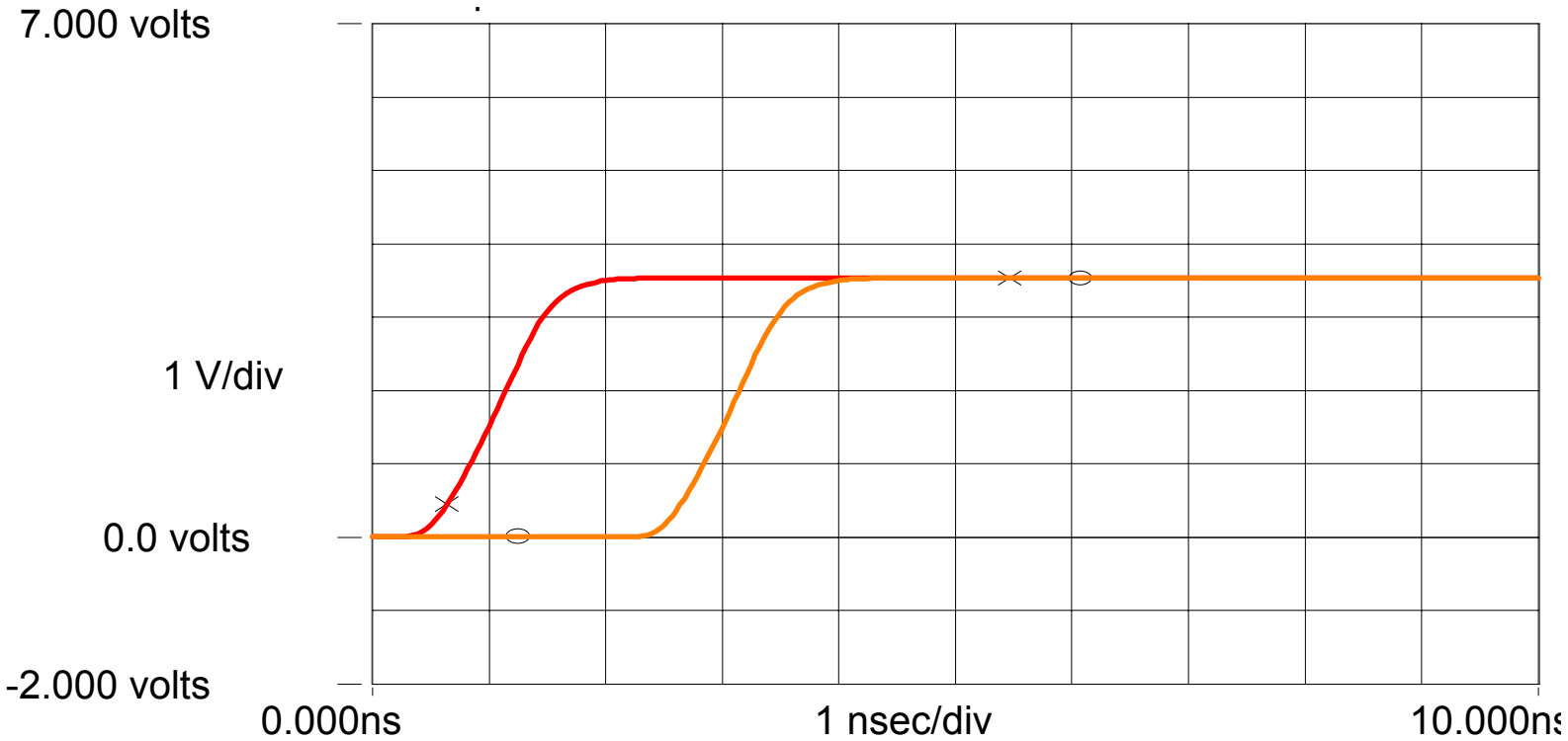
Transmission Line Termination



After Parallel Terminating Rerouted Line

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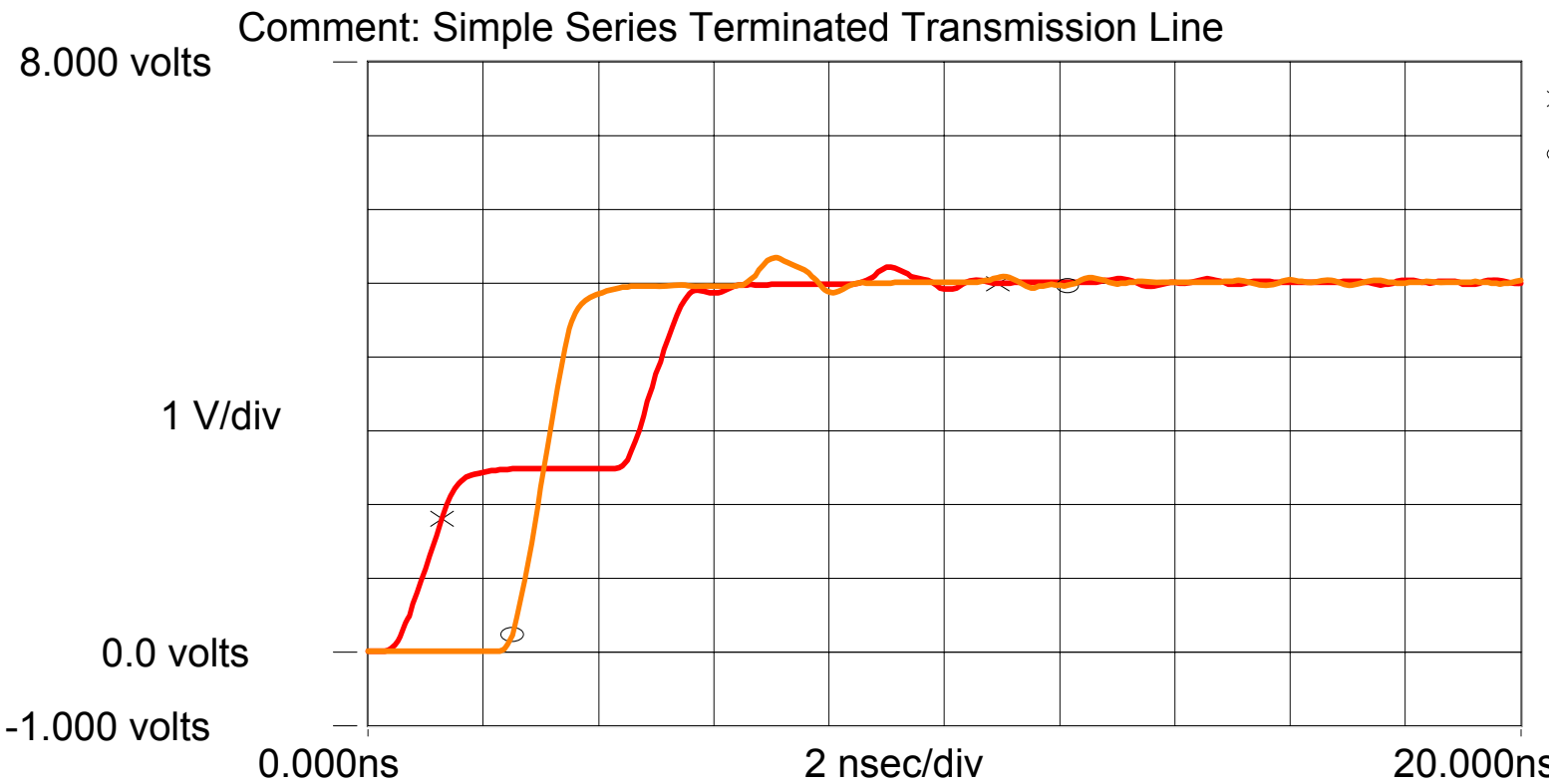
Transmission Line Termination

SERIES RESISTOR

- Must place Resistor within 1/8 Rise Distance of Driver.
- Resistor Value = Zo - Rs(Output Impedance).
- Reflection occurs and is Absorbed back at the Driver.
- Most common w/ Single Load or ALL Loads at end of Line.
- Low-Power Consumption.
- Helps Eliminate Ground Bounce.
- Lowers Power Transients and EMI Dramatically.

Transmission Line Termination



After Series Terminating Rerouted Line

(DO NOT Parallel AND Series Term)

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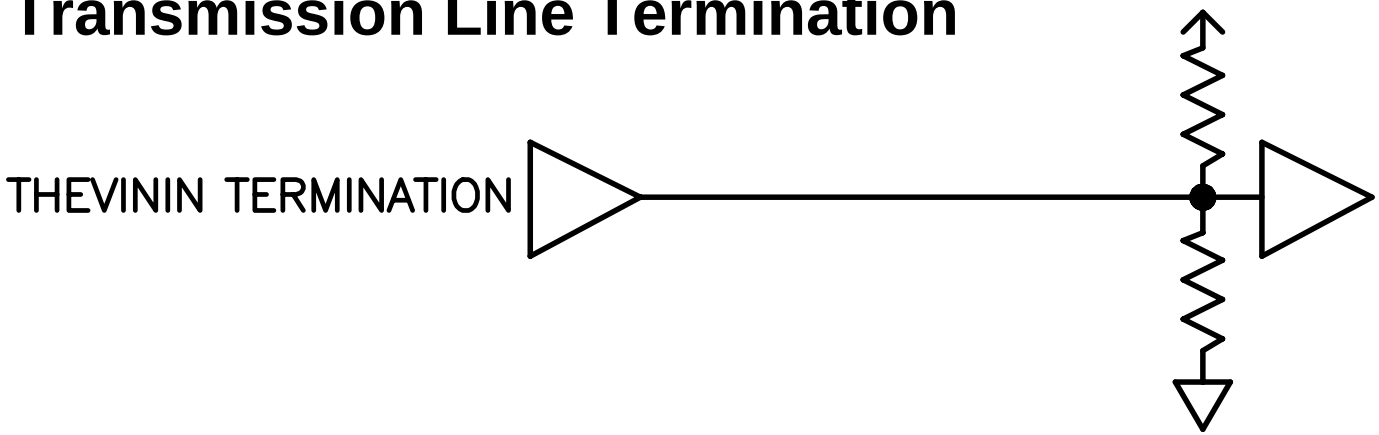
Transmission Line Termination



- Form of Parallel Termination with Two Resistors.
- Useful w/Strong Drivers for Incident Wave Switching.
- Each Resistor tied to Reference Voltage, usually Vcc & Gnd.
- User Defined DC Bias, based on Resistor Values.
- Parallel Combination of Resistors = Zo.
- Requires Twice the Components of most Terminations.
- Resistors Needed at Both Ends of Bidirectional Net.
- Very High Power Consumption (Constant DC Load).

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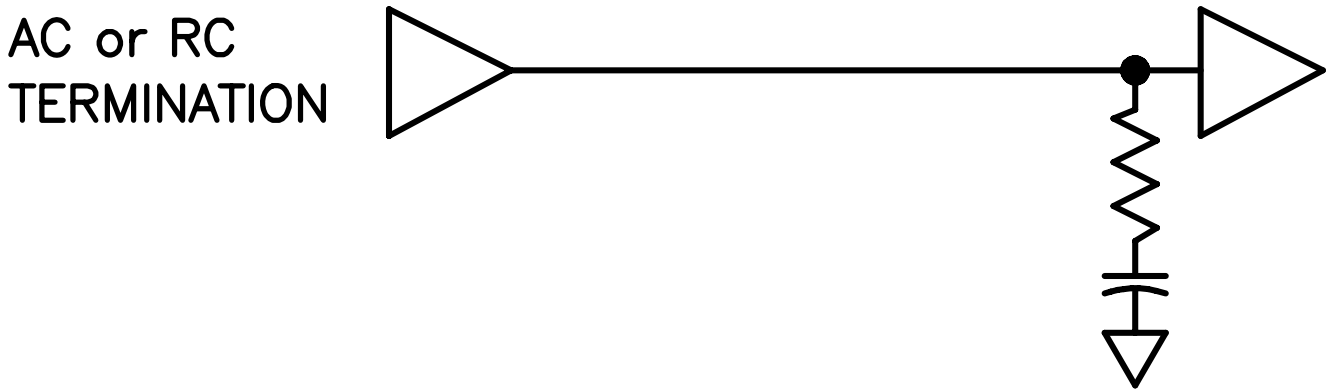
Transmission Line Termination



- Form of Parallel Termination with Small Capacitor added.
- Not Continuous Load. R to Gnd for approx 1xRC Only.
- Solution for Low Power IC that Can't have Series Term.
- Resistor Value = Zo (Strong Driver) / Higher (Weak Driver).
- Capacitor Value - RC = 1.5Tr (Strong Driver).
  C(R+Zo) = 3Tpd (Weak Driver).
- R & C Needed at Both Ends of Bidirectional Net.
- Distorts the Wave of both Rising and Falling Edge.

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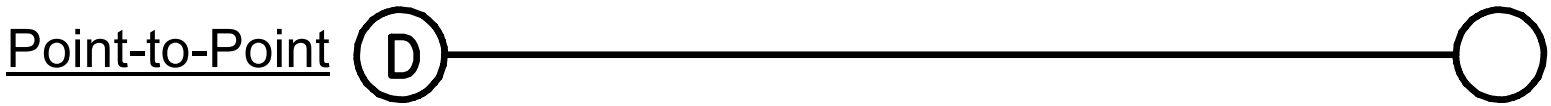
Transmission Line Routing and Termination



- Termination Not Needed IF -
  - Output Impedance is 2/3 Zo or higher. (OR)
  - Line is Shorter than “Max Line Length”.
- When needed, Series Termination is Best.
  - Works whether Single Ended or Bi-directional.
  - No Reflection Mode Delays w/ Single Load.
- Parallel, RC or Thevinin Terminate IF -
  - Logic Family Demands (ECL, BTL, GTL, etc.).

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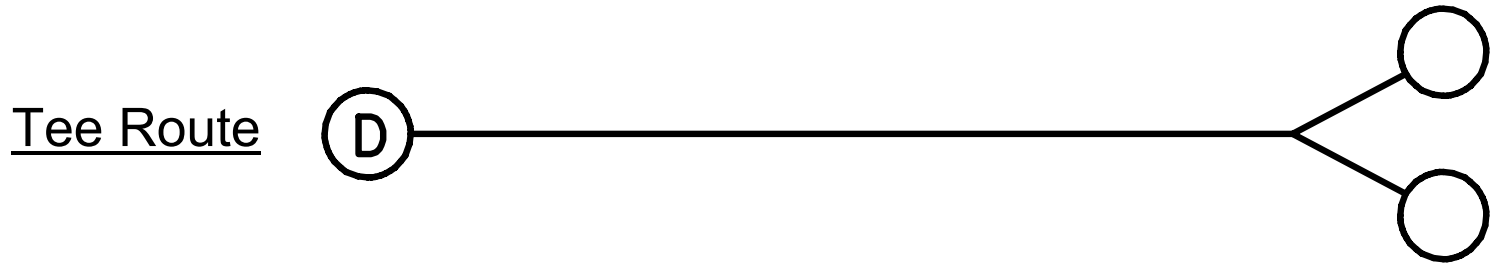
Transmission Line Routing and Termination



- Termination Not Needed IF -
  - Output Impedance is 2/3 Zo or higher. (OR)
  - Line is Shorter than “Max Line Length”.
- When needed, Series Termination is Best.
  - Works whether Single Ended or Bi-directional.
  - No Reflection Mode Delays w/ Loads at End of Line.
- Parallel, RC or Thevinin Terminate IF -
  - Logic Family Demands (ECL, BTL, GTL, etc.).

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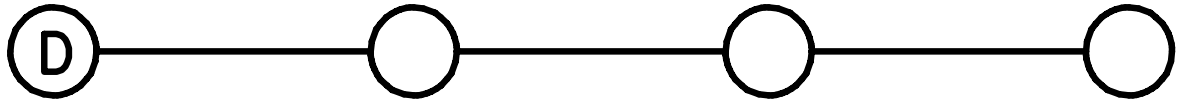
Transmission Line Routing and Termination

Daisy Chain



- Termination Not Needed IF -
  - Line is Shorter Than “Max Line Length”. (OR)
  - Output Impedance is 2/3 Zo or higher. (AND)
  - Driver(s) at one or Both Ends of Line.
- When needed, Series Termination is Best if -
  - Driver(s) at One End or Both Ends of Line.
  - Reflection Mode Delays don’t affect Timing.
- Parallel, RC or Thevinin Terminate IF -
  - Logic Family Demands (ECL, BTL, GTL, etc.).
  - Driver in the Middle of the Line (Terminate Both Ends).

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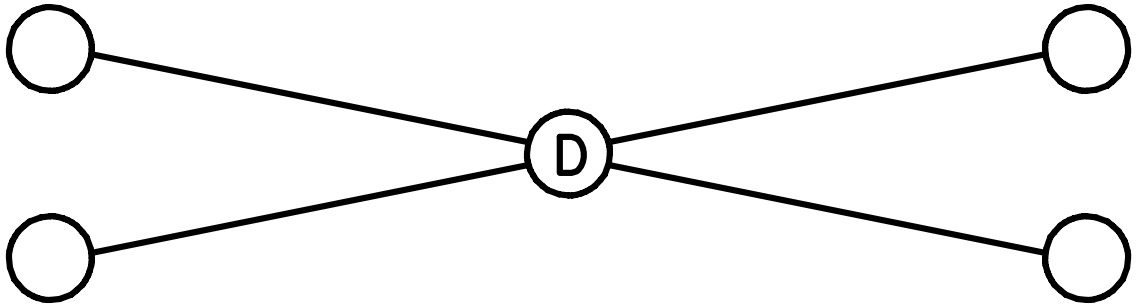
Transmission Line Routing and Termination

Branch by ‘N’



- Used if Loads are Far Apart and -
  - Need to have Incident Wave Switching.
  - (AND/OR) Minimized Skew.
- Requires a Very Strong Driver (Driver Must be able to Source Zo / N).

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Transmission Line Routing and Termination

Branch by 'N' (Cont'd)

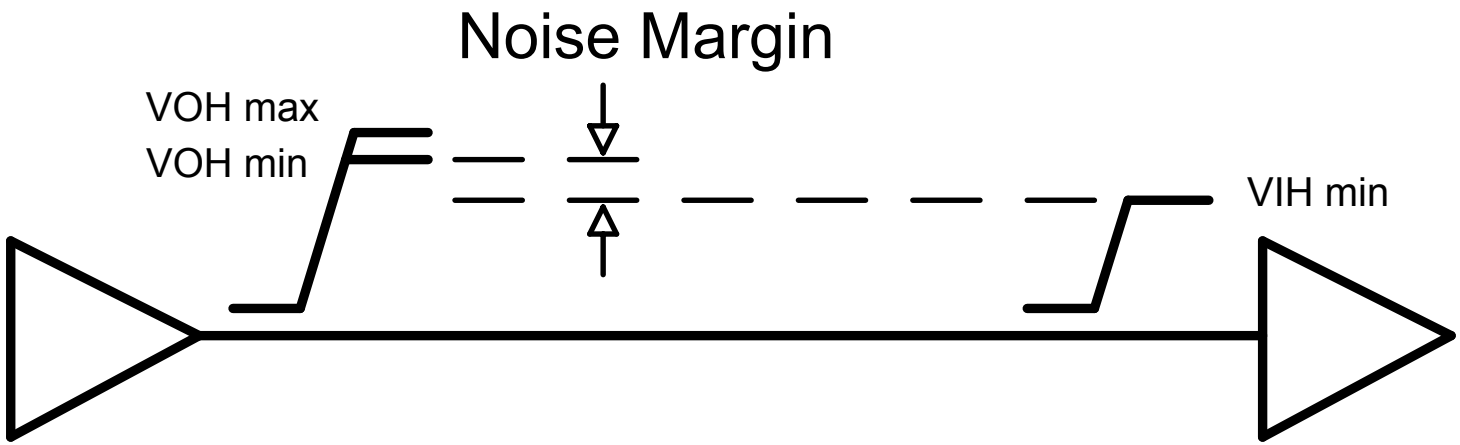
- Termination Not Needed IF -
  - Output Impedance somewhat Matches Zo / N.
  - (OR) Lines Shorter than "Max Line Length".
- Series Terminate -
  - IF Branches are approx Equal in Length.
  - With One resistor equal to Zo / N minus Driver's Output Impedance (Logic Family Dependent) (OR)
  - With 'N' resistors (one for each branch) equal to Zo minus Impedance of Driver.

Signal / Wave Attenuation

1) Reflections - Due to Impedance Mismatch. (Previously Discussed)
2) Signal Cross Talk (Will Discuss).
3) Power Bus (Switching) Noise (Will Discuss).
4) Ground/Vcc Bounce (Ldi/dt Losses).
5) Skin Effect (Resistive Loss in Conductor).
6) Loss Tangent (Property of Molecular make-up of PCB Dielectric).

Signal / Wave Attenuation

= Noise Budget / Noise Margin =



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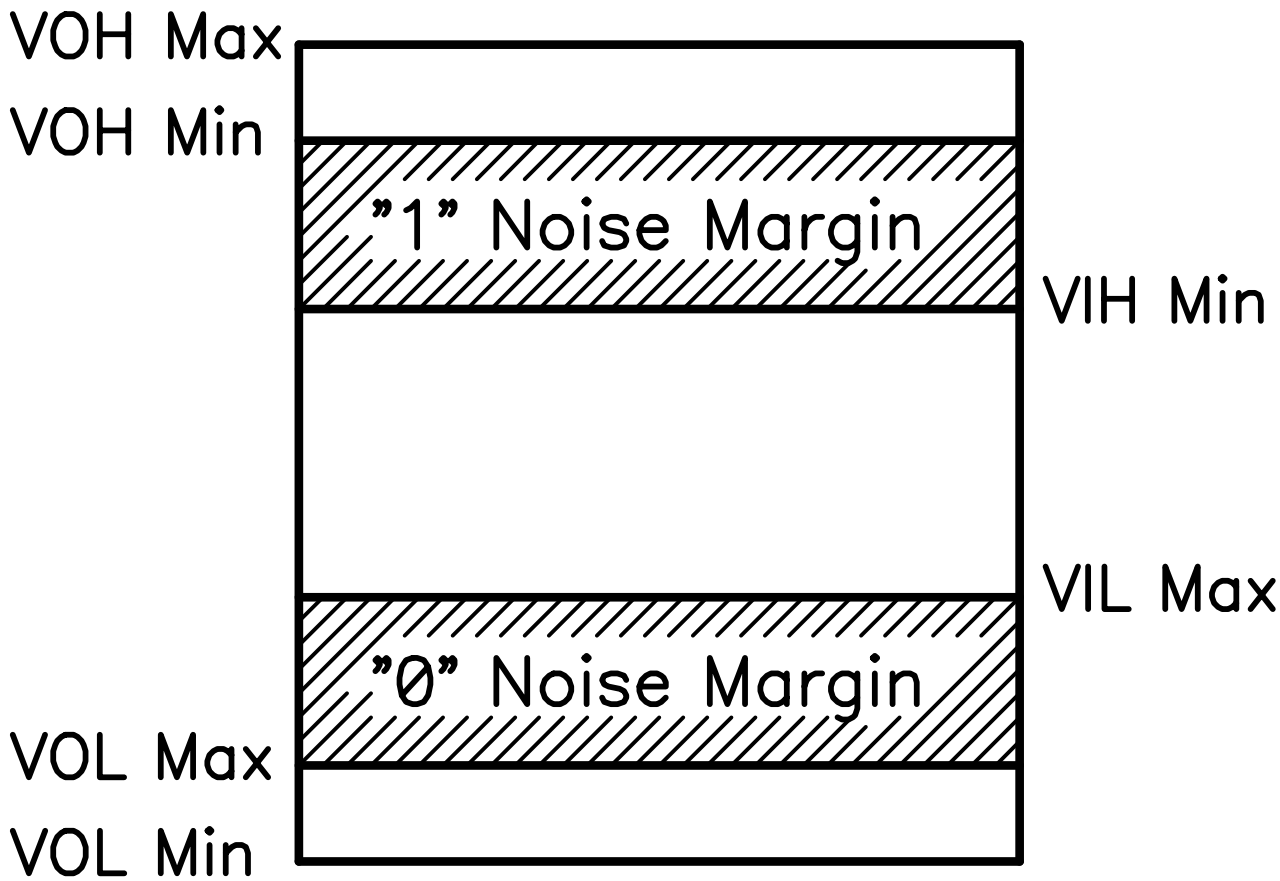
Signal / Wave Attenuation

= Noise Budget / Noise Margin =



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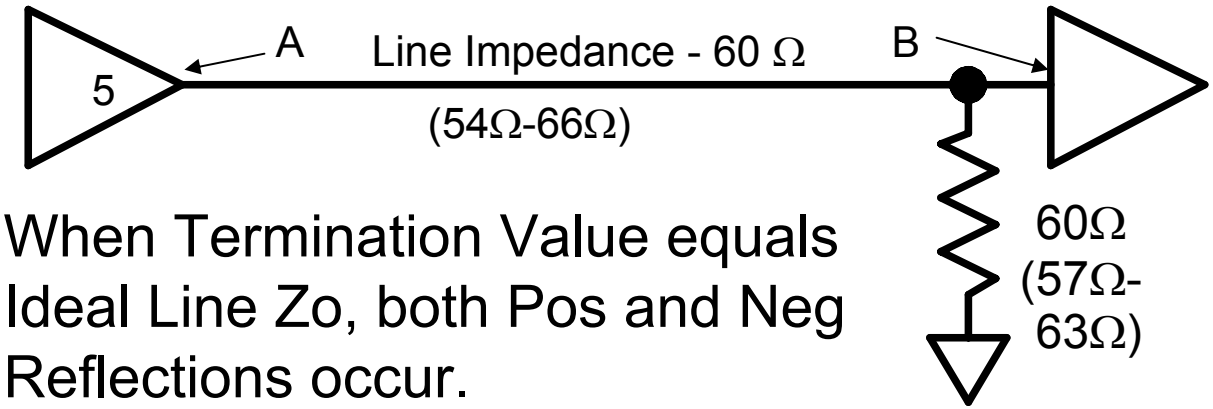
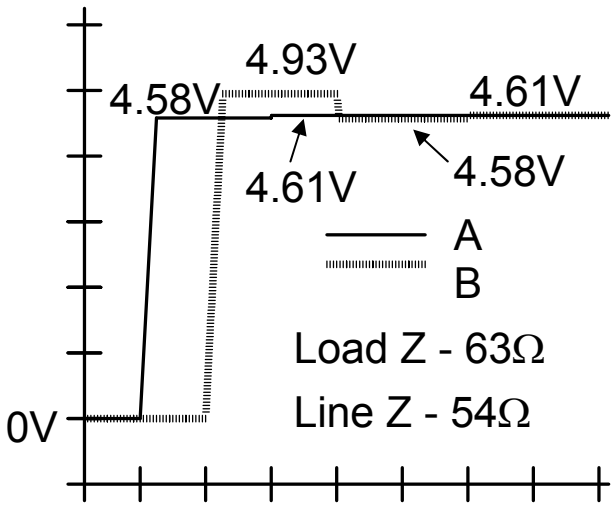
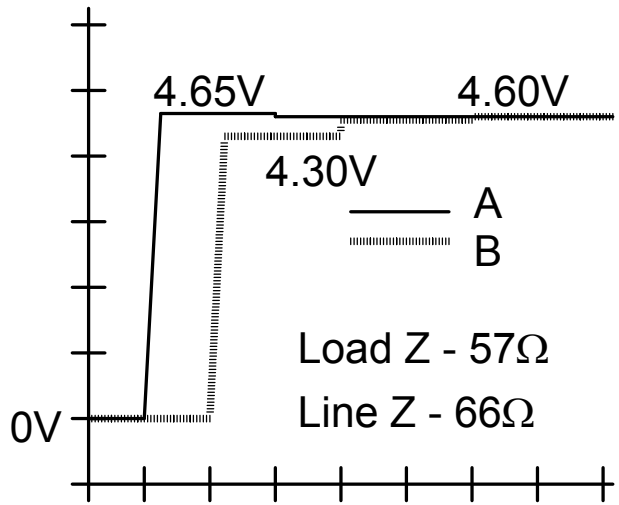
Signal / Wave Attenuation - Reflections



- When Termination Value equals Ideal Line Zo, both Pos and Neg Reflections occur.





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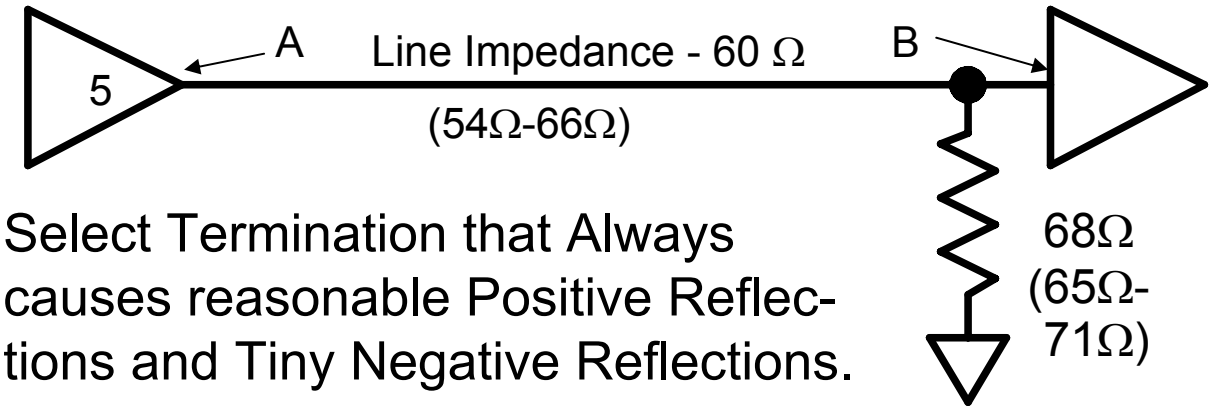
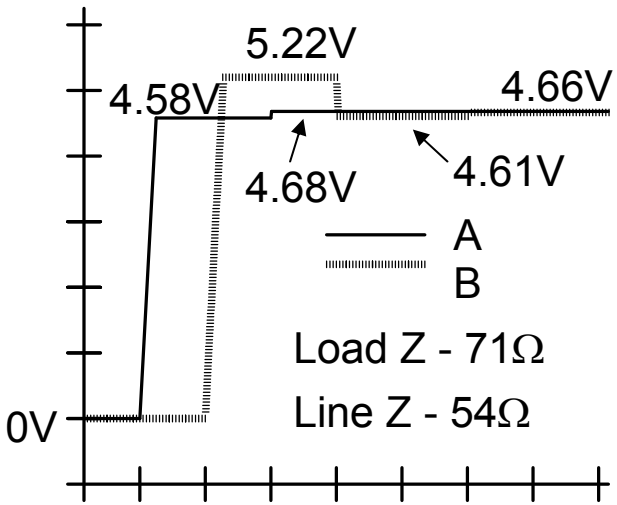
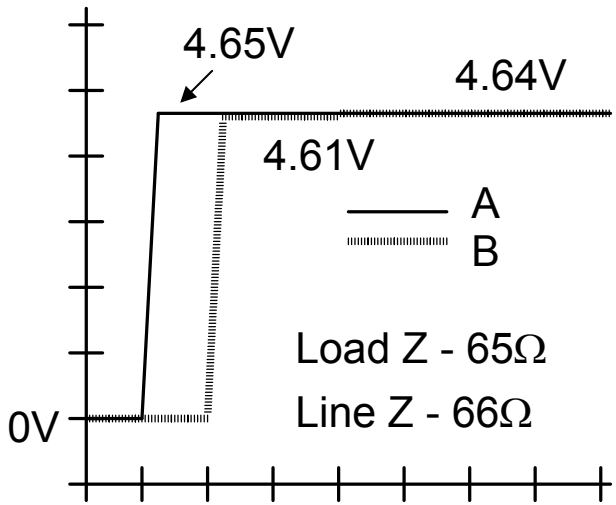
Signal / Wave Attenuation - Reflections



- Select Termination that Always causes reasonable Positive Reflections and Tiny Negative Reflections.





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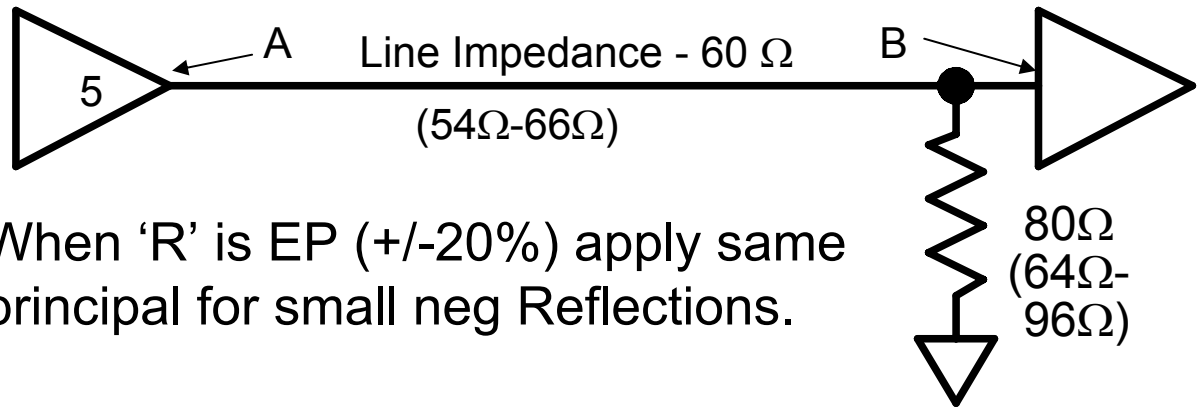
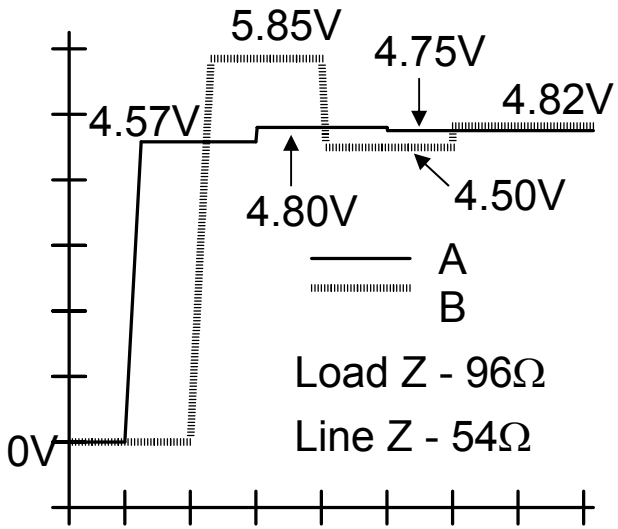
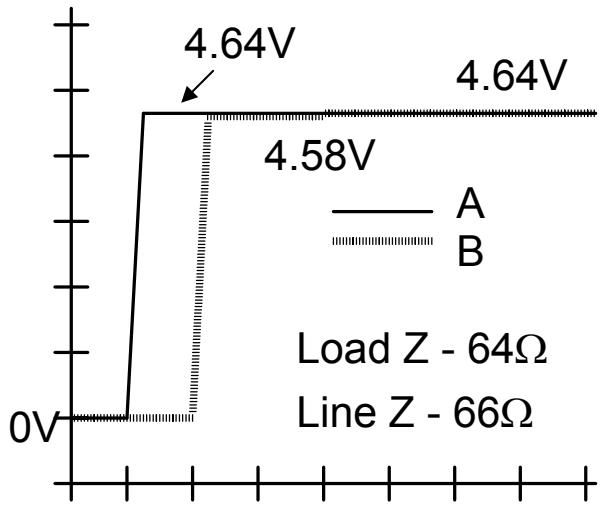
Signal / Wave Attenuation - Reflections



- When 'R' is EP (+/-20%) apply same principal for small neg Reflections.





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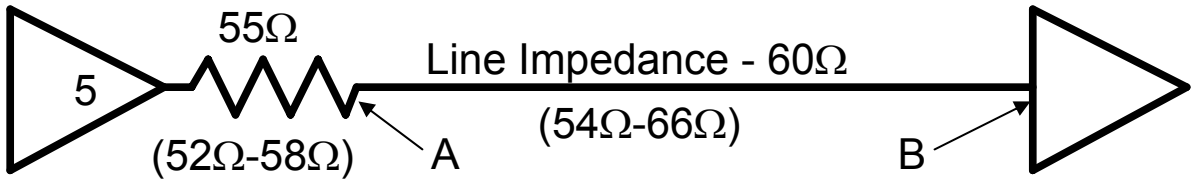
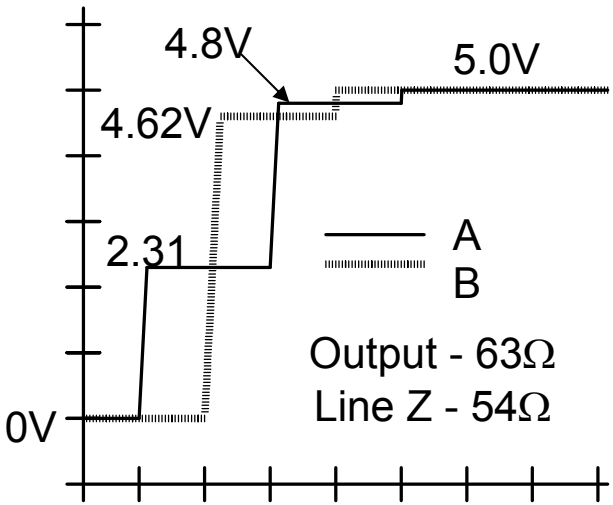
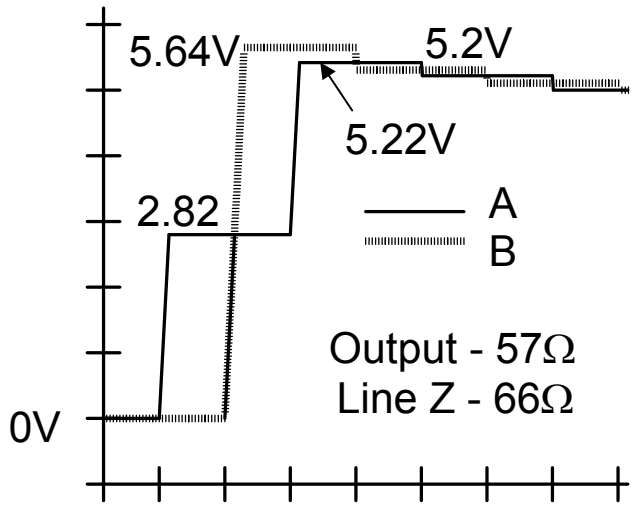
Signal / Wave Attenuation - Reflections

- When Termination Value + Output Z equals Ideal Line Zo, small Pos and Neg Reflections occur.







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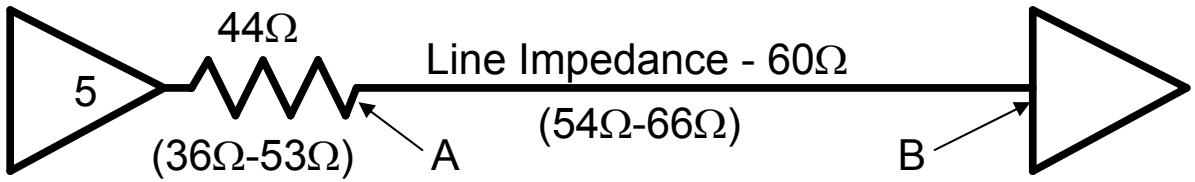
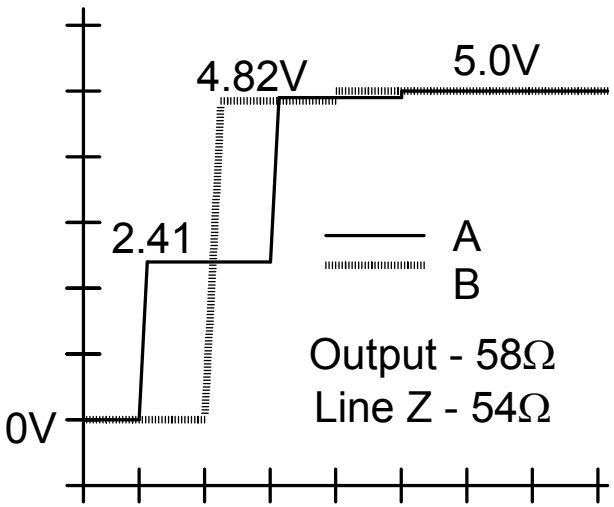
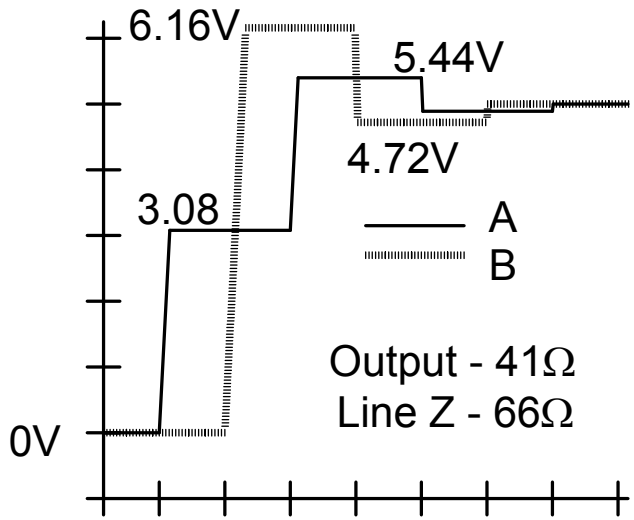
Signal / Wave Attenuation - Reflections

- When ‘R’ is EP (+/-20%) select value that creates larger pos reflections and Small neg reflections.







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Ground or Vcc Bounce-

- Results when Very Fast Switching Currents cause a Voltage Drop across the Power or Ground pins of an IC.

$$V = L di/dt$$

Where: L = Inductance of IC Pin(s)

di = Current Needed to Charge or Discharge Transmission Lines.

dt = Rise Time or Fall Time of IC.

Ground or Vcc Bounce-

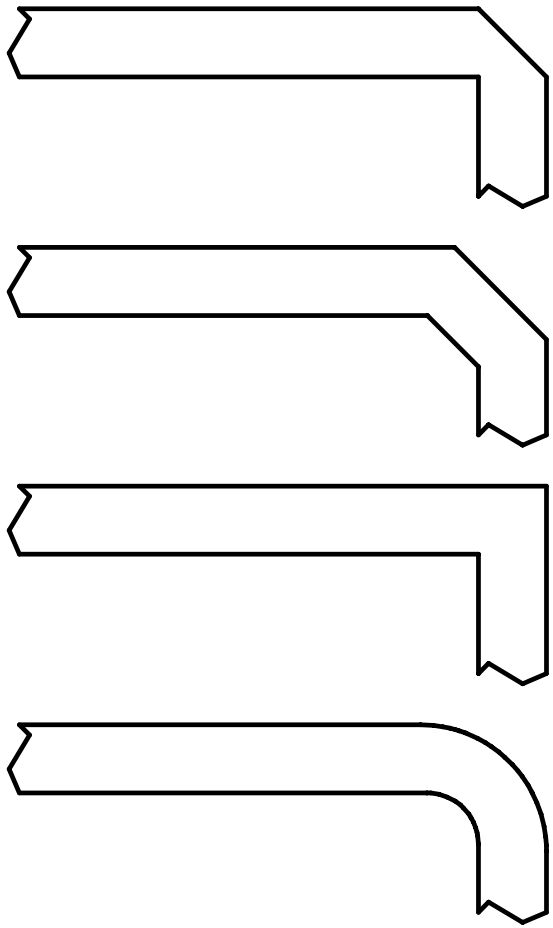
- The large Voltage Drop causes Power in the IC to Fall Below a Minimum Acceptable Level or for 0v (Ground) in the IC to Raise Above a Maximum Acceptable Level.
- Remedies -
  - Low Inductance Lead Frame ICs.
  - Multiple Power and Ground Pins in IC Lead Frame.
  - Very Short Power and Ground Paths
  - Proper Location of Power / Ground Vias.
  - All of the Above.

Sample Vcc Bounce Calculation -

1) 50ma drive current / Memory Line X 32 lines = 1.6 Amps.
2) 30 Power Pins (Memory) @ 12nH per pin = .4 nH total.
3) Z of pins = $2\pi FL$ = 6.28 x 100MHz x .4nH = .251 ohm.
4) .251 (Pin Z) x 1.6 Amps (item 1) = .40V drop across pins.
5) 3.3V (Vcc) - .40V (item 4) = 2.90V, minus 200mV internal V drop within 8245 IC = 2.7V(Vcc) left to drive Memory.
6) 2.7V (item 5) into 6 ohm (min 8245 output Z) to 50 ohm (Trace Zo) Voltage Divider = 2.39V Incident Wave.
7) Vin High Min for 8245 PowerPC is 2.0 V, leaving Noise Margin = 390 mv.

What if Crosstalk, Power Bus Noise & Reflections add up to more than 390 mv??????

Attenuation- PCB Trace Corners



90 Degree Corner,
Cut at 45 Degrees.

45 Degree Corner.

90 Degree Corner.

Radius at Corner.

Which of these is BEST?

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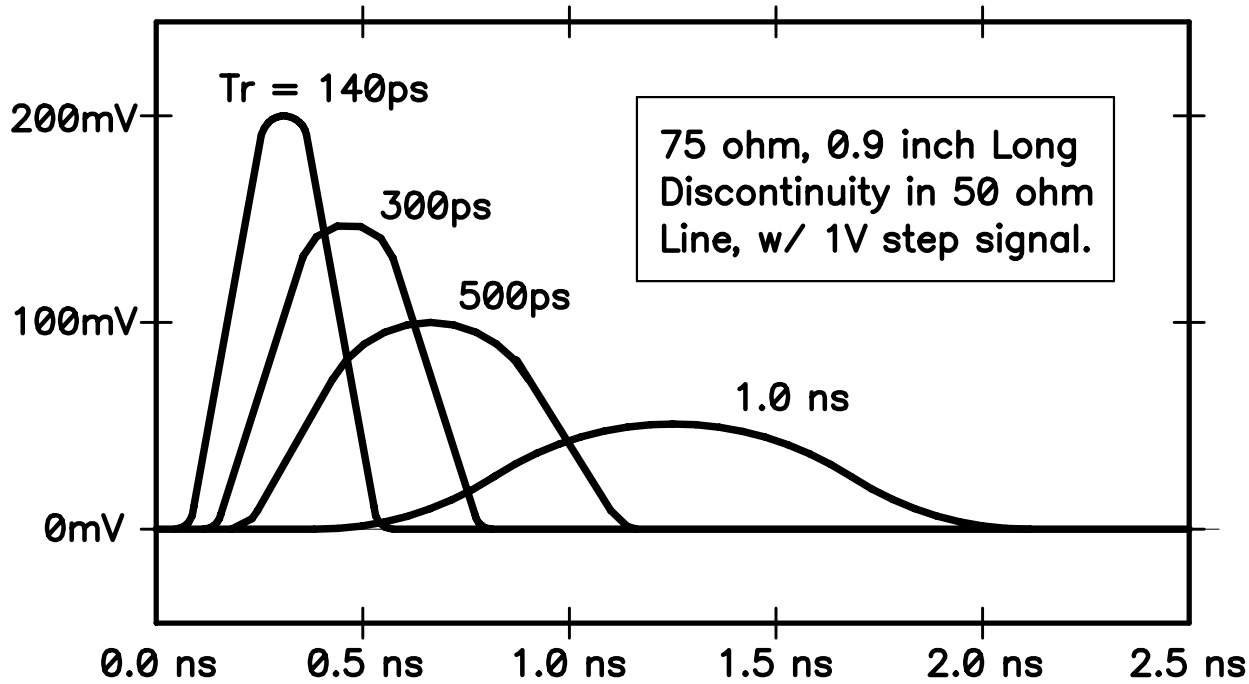
- Reflection Amplitude vs Rise Time -

- Per given Length of Discontinuity, Amplitude of a Reflection is a Function of Rise Time.



(Info from Speeding Edge, Spring 2001)

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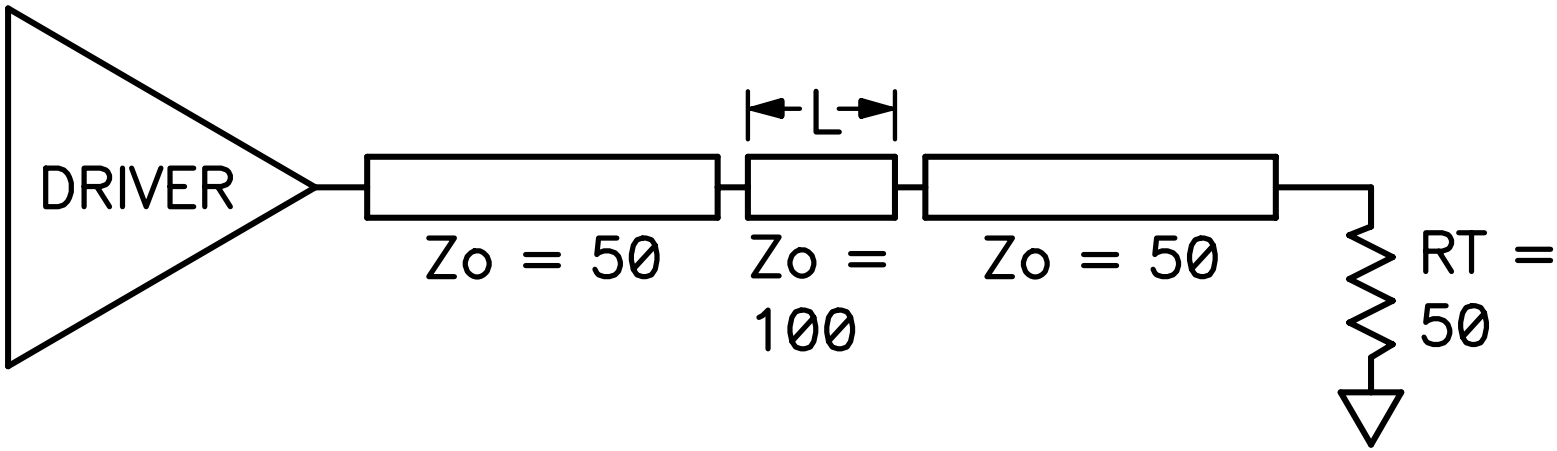
- Reflection vs Discontinuity Length -

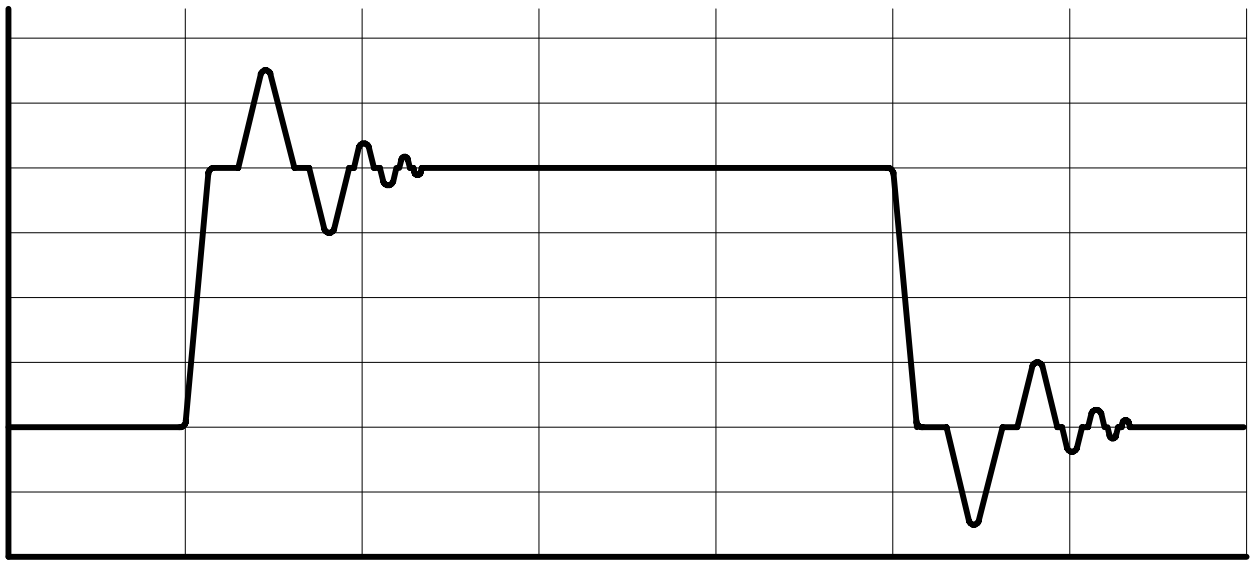
- Said Another Way- Per given Rise Time (i.e.- 1.0ns), Amplitude of a Reflection is a Function of Discontinuity Length.



- From the % Reflection Equation, 2 Reflections occur, One Positive and One Negative.

- Reflection vs Discontinuity Length -

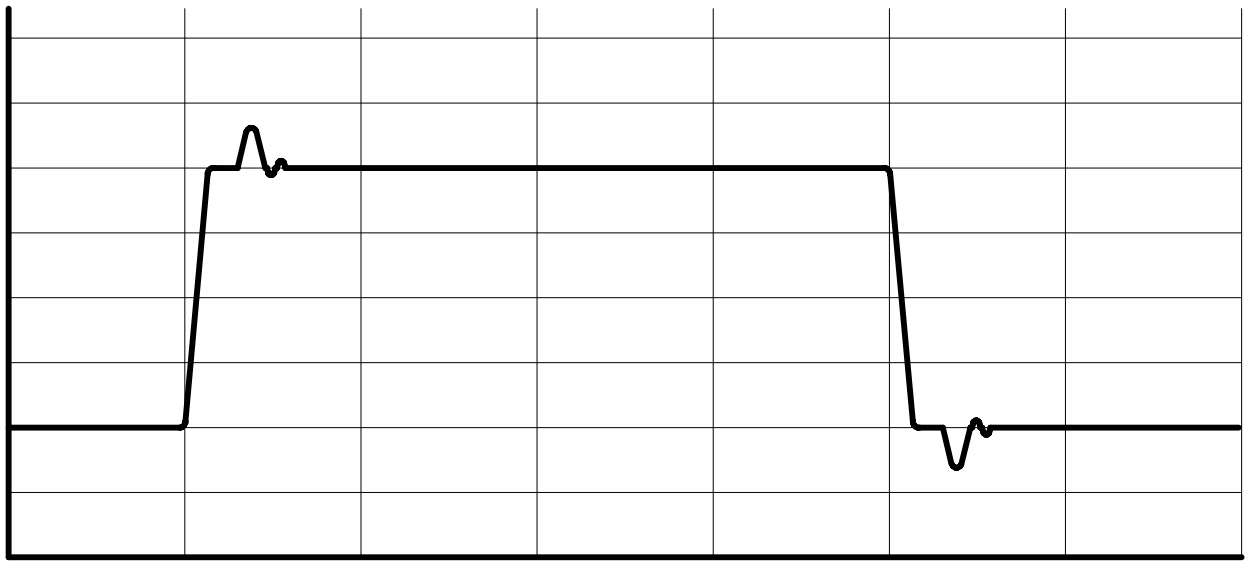
- If ‘L’ is At or Beyond 1/4 of Rise Distance, Reflections reach Maximum Size.
- Reflections from 1.0 ns Signal, w/ ‘L’ at 4.0”.



- Signal at first 50 ohm Segment and middle of Discontinuity.

- Reflection vs Discontinuity Length -

- If ‘L’ is Less than Signal Critical Length, the Reflections (Opposite Polarity to one another) begin to Cancel.
- Reflections from 1.0 ns Signal, w/ ‘L’ at 1.0”.

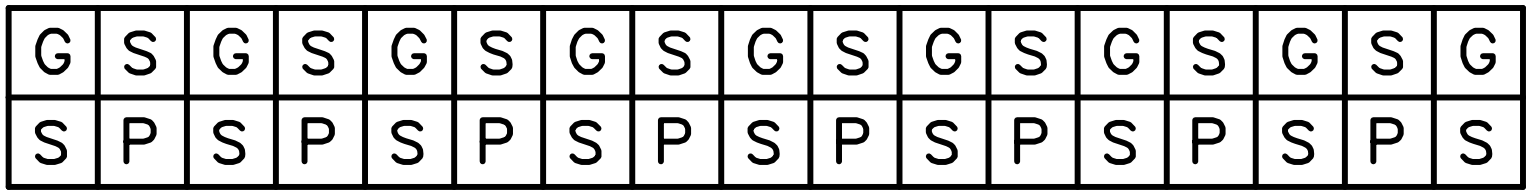


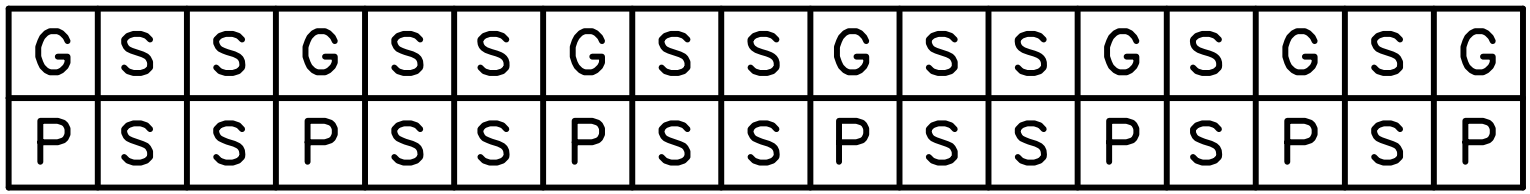
- Average Via is .062” Long (Reflection is .5%).

- Conventional Connectors -

- Connector Assignments should be:

- Best





- OK

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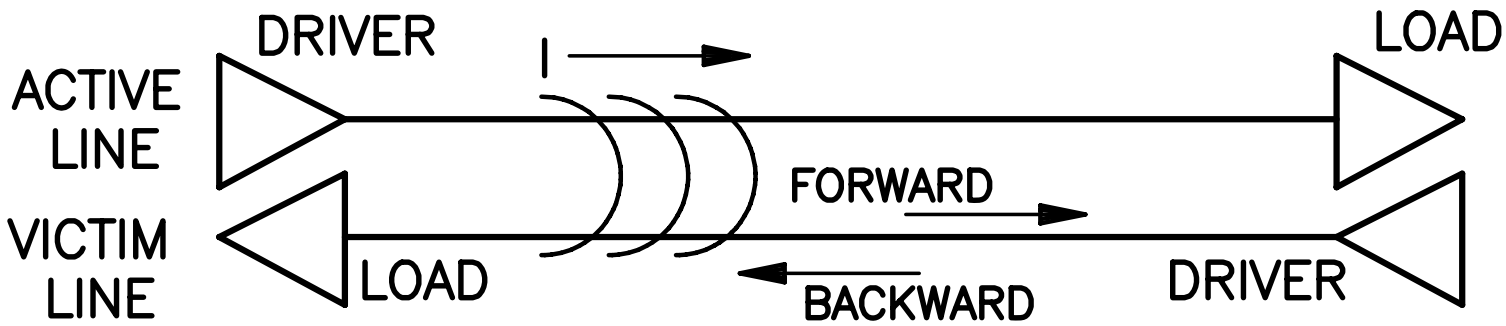
Cross Talk

- Transfer of Pulse Energy from an Active Source Line to a Passive Victim Line.
- Coupled Capacitively, Inductively or Both.
- Cross Talk occurs when Signal Traces route in Parallel for an extended distance, Side-by-Side or on Adjacent Layers.
  - Adjacent layer parallelism is Much Worse.
- Increases, per given Trace Length, as Tr Increases.

Cross Talk

- Takes Two Forms - Forward and Backward.



- Forward Cross Talk requires Extremely Long parallel runs to create Problem in Victim.
- Backward Cross Talk Rises Rapidly. Reaches Max in slightly more than 1/2 Rise Distance.

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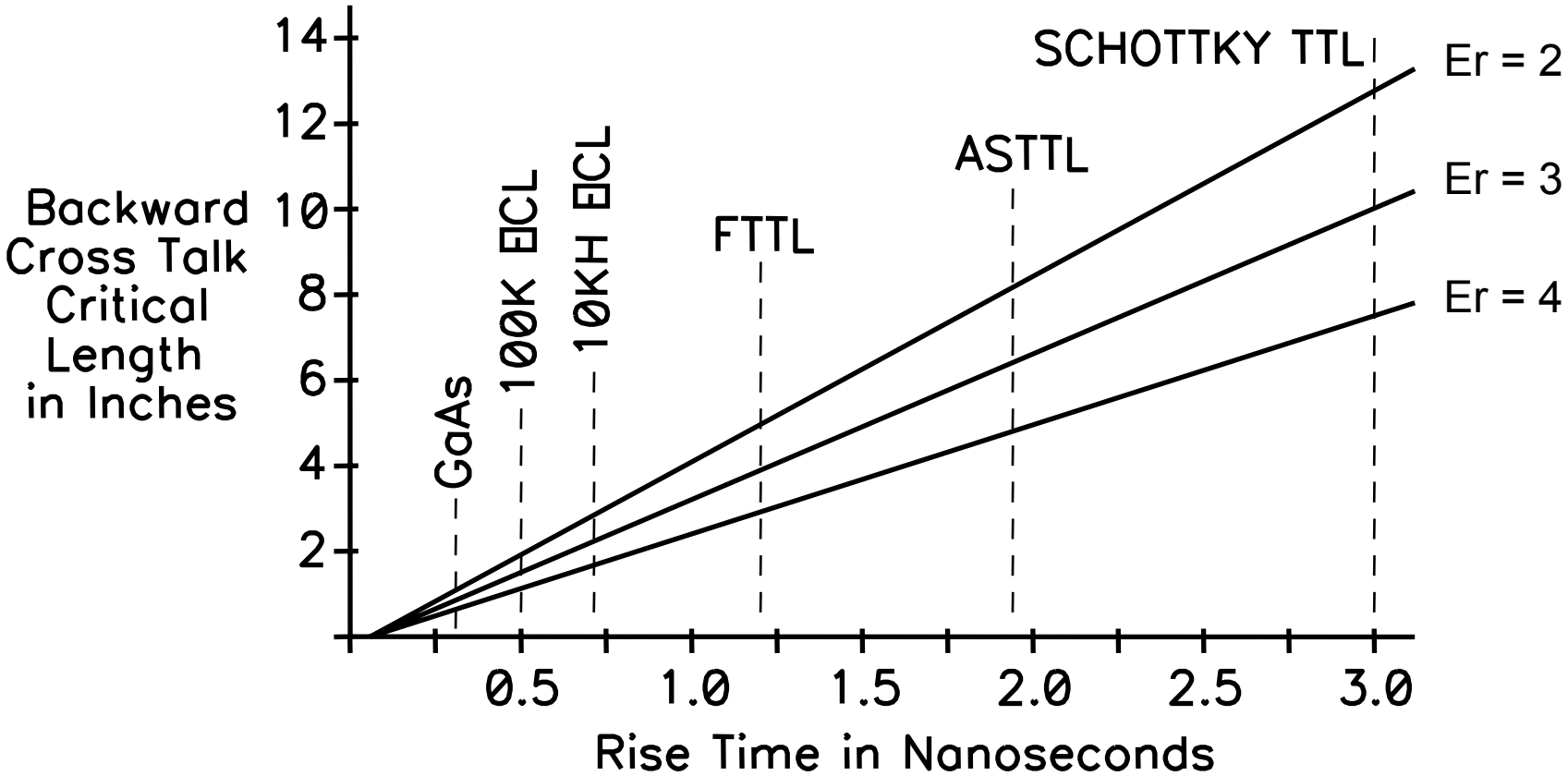
Cross Talk

- Forward Cross Talk -
  - Coupled Pulse Width equals Tr of the Signal of the Coupling Line.
  - Takes Parallel Runs of 4 to 6 Times Rise Distance to Couple enough Energy to cause a Problem.
  - Coupled Pulse Amplitude grows until it's equal to Amplitude of Signal from Coupling Line.
  - Coupled Pulse is the Opposite Polarity as Signal from the Aggressor Line.

Cross Talk

- Backward Cross Talk -
  - Coupled Pulse Width equals 2 x Propagation Time of Parallelism.
  - Coupled Pulse Amplitude rises until Parallelism equals ‘Cross Talk Critical Length’.
  - Then, Coupled Pulse Levels off and gets Wider.
  - Amount of Coupling in ‘Xtalk Critical Length’ is a function of Separation vs Height above Plane.
  - Coupled Pulse is the Same Polarity as the Signal from the Aggressor Line.

- Backward Cross Talk Critical Length -

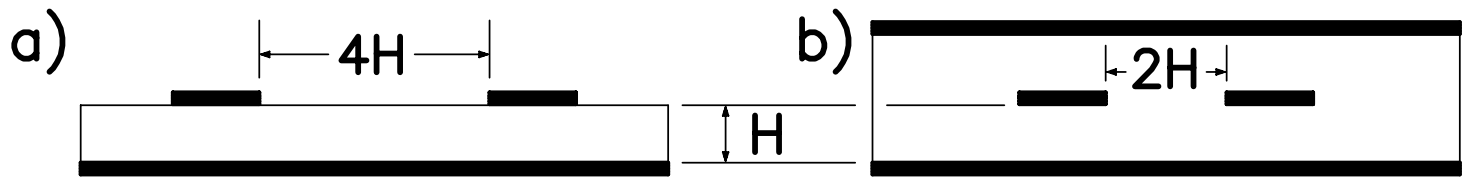


- Backward Cross Talk -

- Other factor is how Far Apart 2 Traces Route vs. Distance to Plane(s) (In Like Logic Family).

Ideal Microstrip

Ideal Stripline



- At this Spacing, Malfunction is unlikely to Occur on even the Most Sensitive Digital Signals .

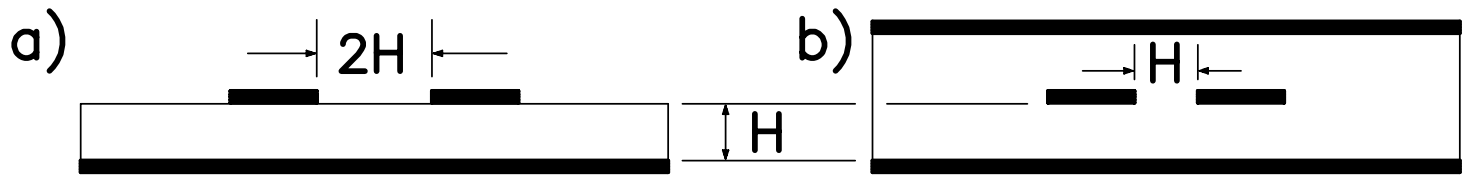
(But how Realistic is this Spacing?)

- Backward Cross Talk -

- In the Real World, 4H and 2H Separations are Highly Unlikely, in all but a Few Situations.

Realistic Microstrip

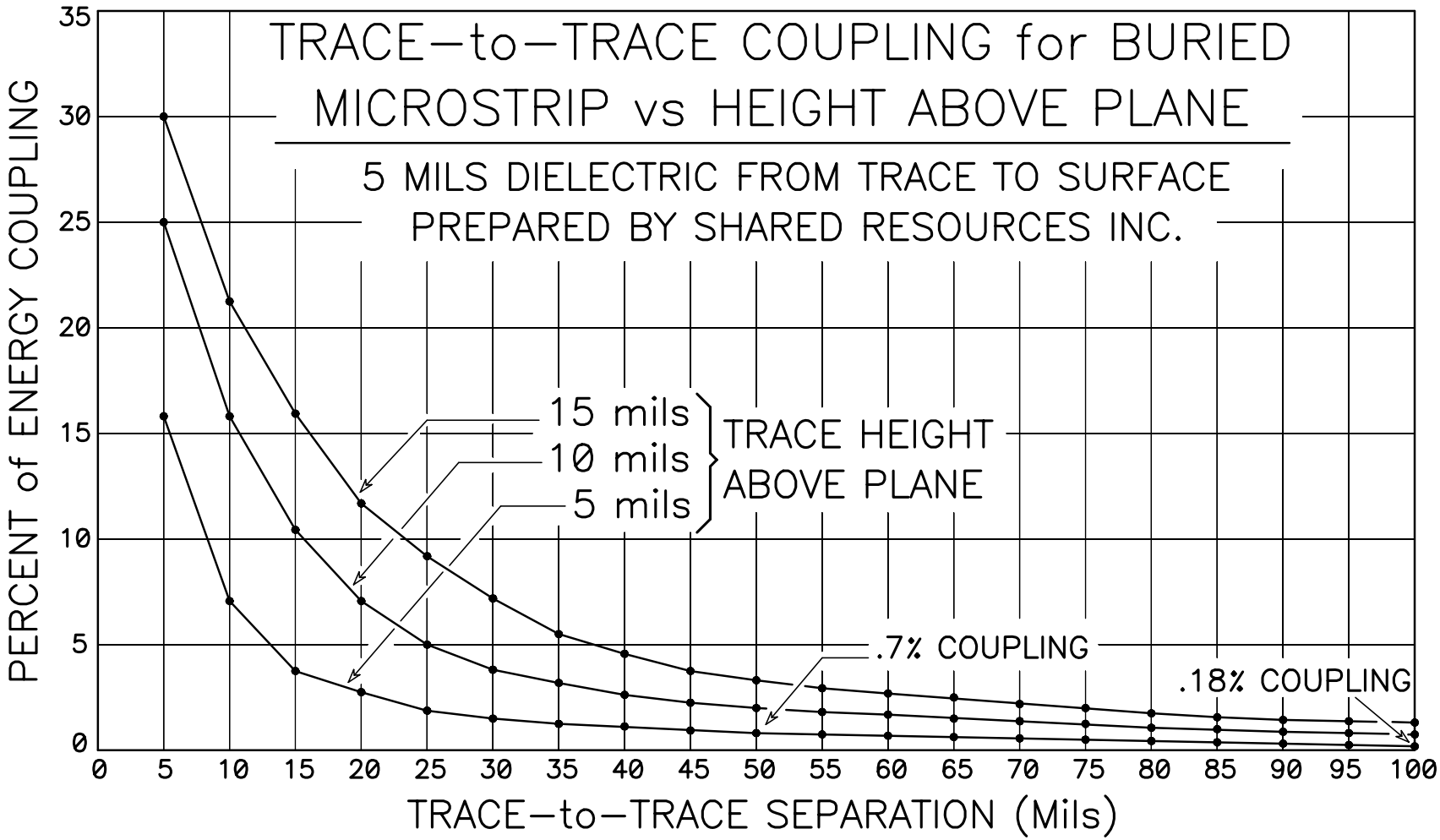
Realistic Stripline



- Amount of Coupling (Approx 10%) Generally will Not be enough to cause Malfunction.

(Within Like Logic Families!!!)

- Backward Cross Talk -



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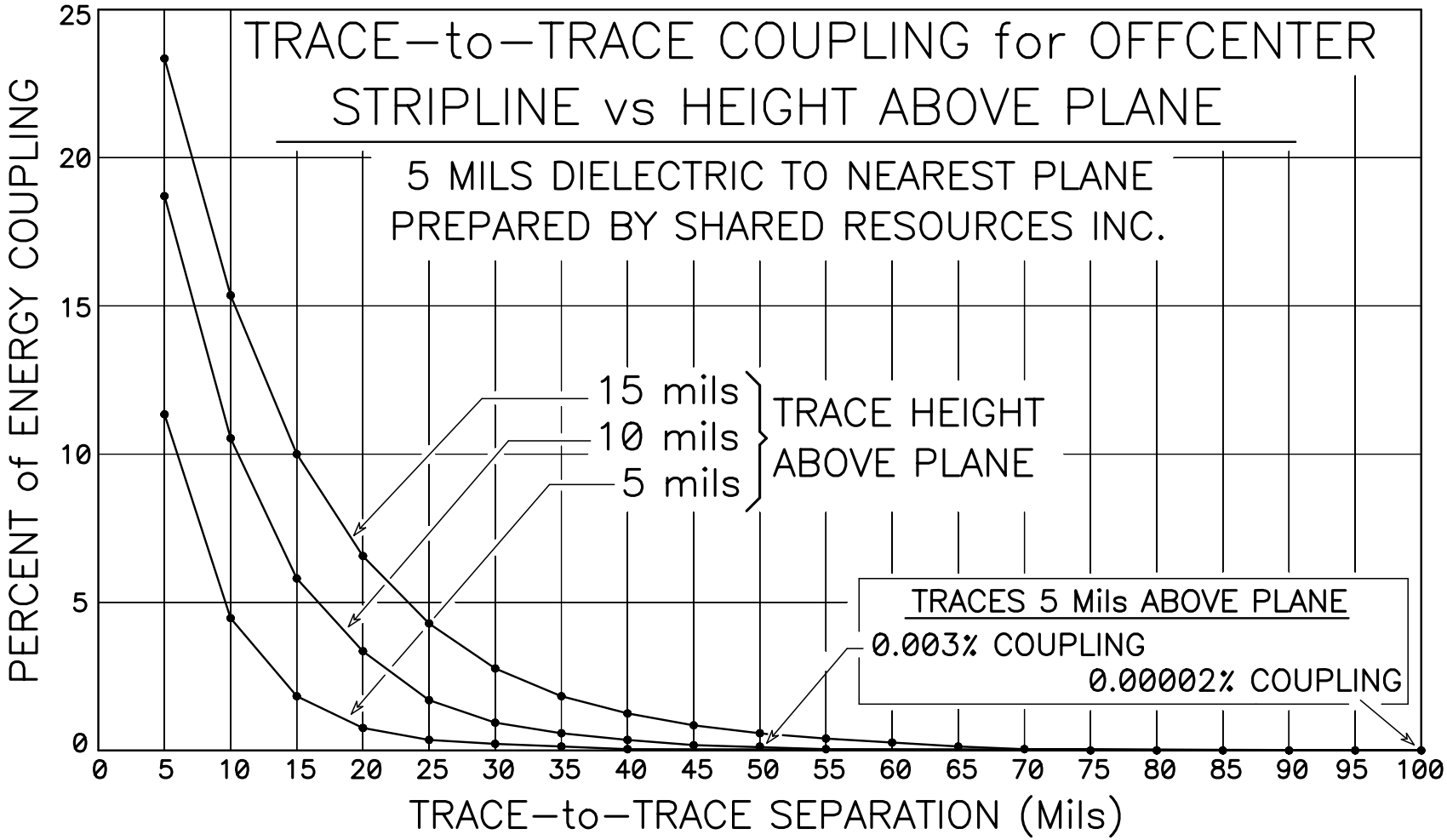
- Backward Cross Talk -



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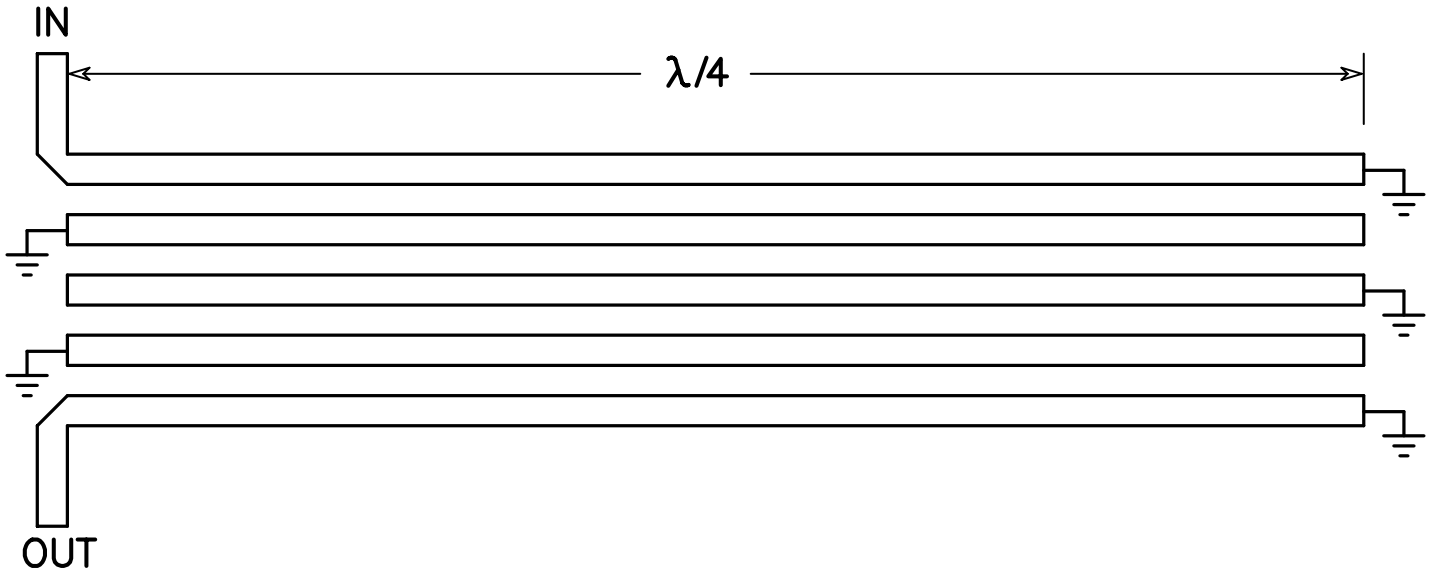
- Guard Traces -

- On Single or Double Sided PC Board:
  - Critical Routes- Self and Loop Inductance are Dramatically Improved.
  - Guard Trace to Route Parallel to Critical Trace, Same Layer.
  - Connect to Ground at Driver and Receiver.
  - Ground at ONE End Only is Electrostatic Shield ONLY.
- **No Real Benefit On Properly Structured Multi-layer Digital PC Board.**

- Guard Traces -

Bandpass Filter made from Strips of Copper.



Side by side traces, such as “Guard Traces” can inadvertently enhance coupling by creating a band pass filter. Traces, no matter how their ends are connected to underlying planes, are LC networks that resonate at some frequency.

Electro-Magnetic Interference (EMI)

- EMI is that condition where a Circuit or System has sufficient Radiated or Conducted Energy to interfere with performance of other Circuits or Systems.

- EMI is the Transfer or Coupling of Pulse Energy from an active Circuit or Signal Source to a less active Victim Circuit.

Control of Electro-Magnetic Interference (EMI)

- All Circuits have CM Noise caused by Voltage Drops across inductance in circuit elements and Stray Magnetic Fields in Finite Current Loops -
  - In Power / Ground Bus.
  - Across Circuit Traces
  - In IC Pins & Interposer Boards in IC Pkg.
  - Across Connector Pins
  - etc.

Types of Electro-Magnetic Interference (EMI)

- Electro-Magnetic Energy can exist in Two forms:
  - Differential Mode.
  - Common Mode.

- The Difference becomes easier to understand when thinking in terms of Current Flow, instead of Voltage.

Types of Electro-Magnetic Interference (EMI)

- EMI- Differential Mode -

- An IC sends a Current down a trace, an Equal Current is returned to driver / All received at Load.
- These Equal Currents, traveling in Opposite Directions, are Differential Mode Operation.
- Since a PCB only emulates a Coax, complete E-field and H-field containment is Not possible.
- Radiating Stray fields are Differential Mode EMI.

Types of Electro-Magnetic Interference (EMI)

- EMI- Common Mode -

- Caused by Common Mode Current-
- CM is Unwanted Current, flowing in Common Direction, through Unintended Paths.
  - Signal Not Paired Directly with an Equal and Opposite Current.
  - Voltage Transients Generated on Power / Ground Planes (V = Ldi/dt).
- CM Noise is usually Common to Several Conductors.

Types of Electro-Magnetic Interference (EMI)

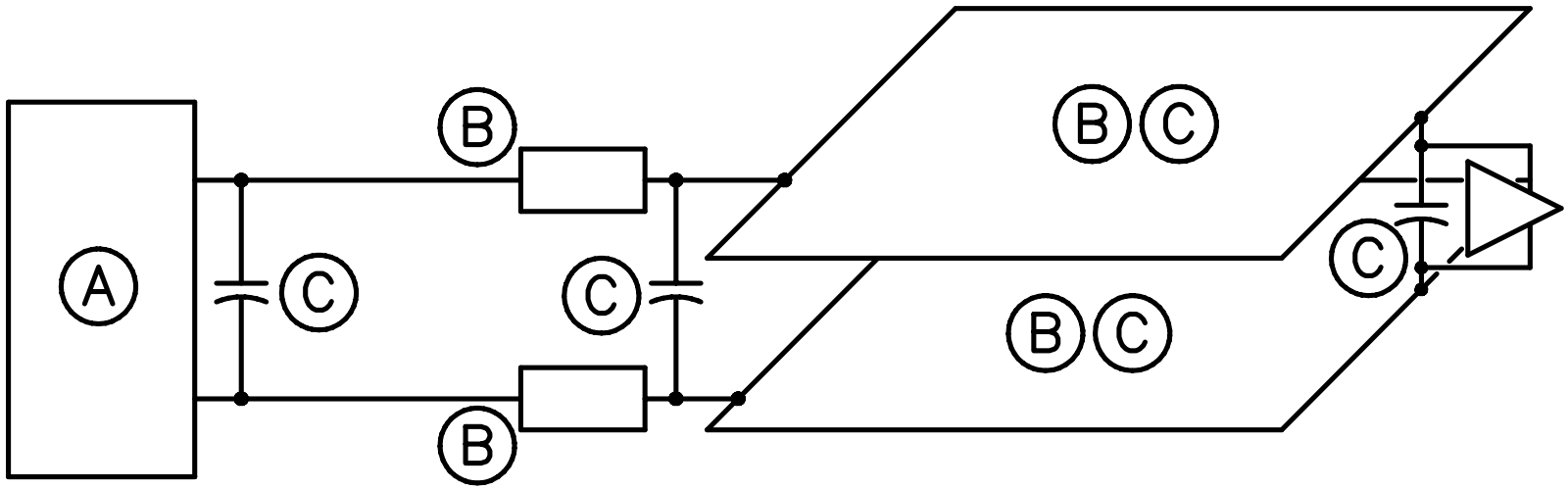
- EMI- Common Mode -

- Keys to Control Common Mode EMI-
  - Proper Use and Location of Planes.
  - Correct Decoupling of Power Currents.
  - Control Return Currents w/ Layer Pair routing.
  - Control Amount and Rate of Current from IC Output Stages.
  - Proper Component Selection.
  - Provide Proper RF Shielding of the System Case and/or Proper RF Ground.

Power Distribution System

- Design feature of PC Board with enormous impact on output Signal Integrity & EMI.
- The Foundation of the ‘Building’.
- If Power System fails to provide Current to Output Stages at any Frequency in spectrum-
  - Transients Develop and EMI risk severely increases.
  - IC Rising / Falling Edges can be distorted, creating Non-Monotonic Signals.

Power Distribution System



- If Output Tr is 1.0 ns, Power System Must Deliver Energy to Output Stage of IC in 1.0 ns.
- Power to Drive IC Output Cannot come from Power Supply directly, due to Inductance.
- Frequency of Power is from ‘Clock’ to ‘.50/Tr’.

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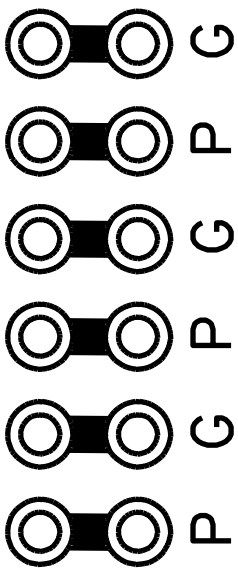
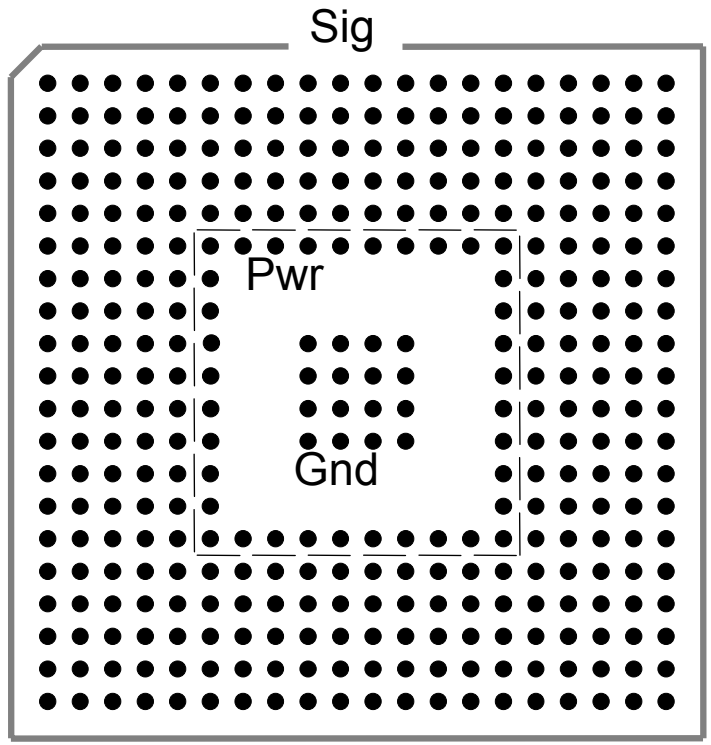
Power Path - Power Distribution System

Dual Row Connectors.



What about IC Lead Frame Inductance?



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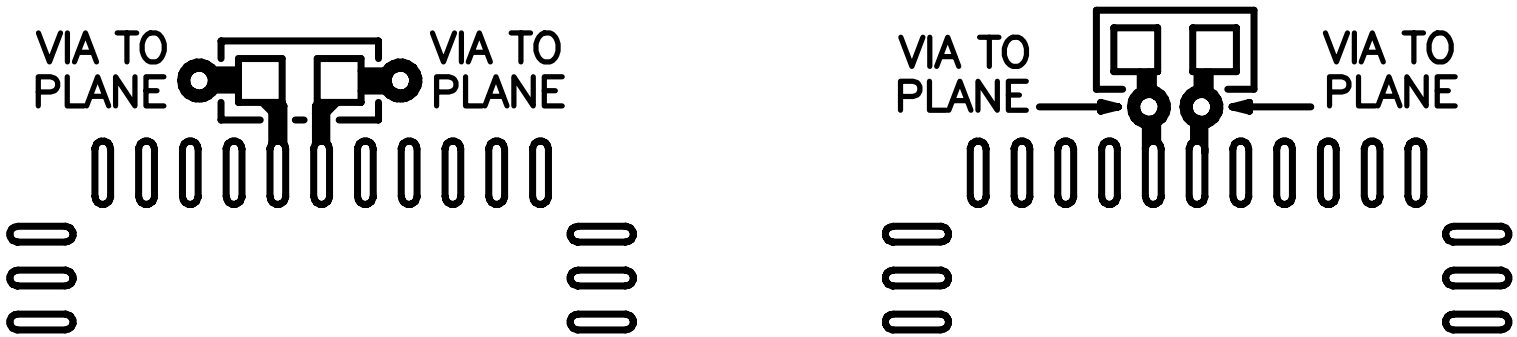
Decoupling - Power Distribution System

- Due to Inertia, Power Supply can't respond Rapidly to Demands for Current to ICs.
- Power System Capacitance (High Frequency Tank of Energy) Provides High Speed Current until Power Supply can respond.
- Multiple Harmonics Require -
  - Power Bus Capacitance be high at broad range of Frequencies.
  - Power Bus Inductance MUST be Low.
  - Power Bus Impedance MUST be VERY Low.

Decoupling - Power Distribution System

Usual Connections for Decoupling-

- One Cap per Pair of Power & Ground Pins???
- Large Vias???



- **If Cap to IC distance greater than .125”, Via Cap and IC directly to Planes.**
- Which is Best? Is either Ideal or Necessary?

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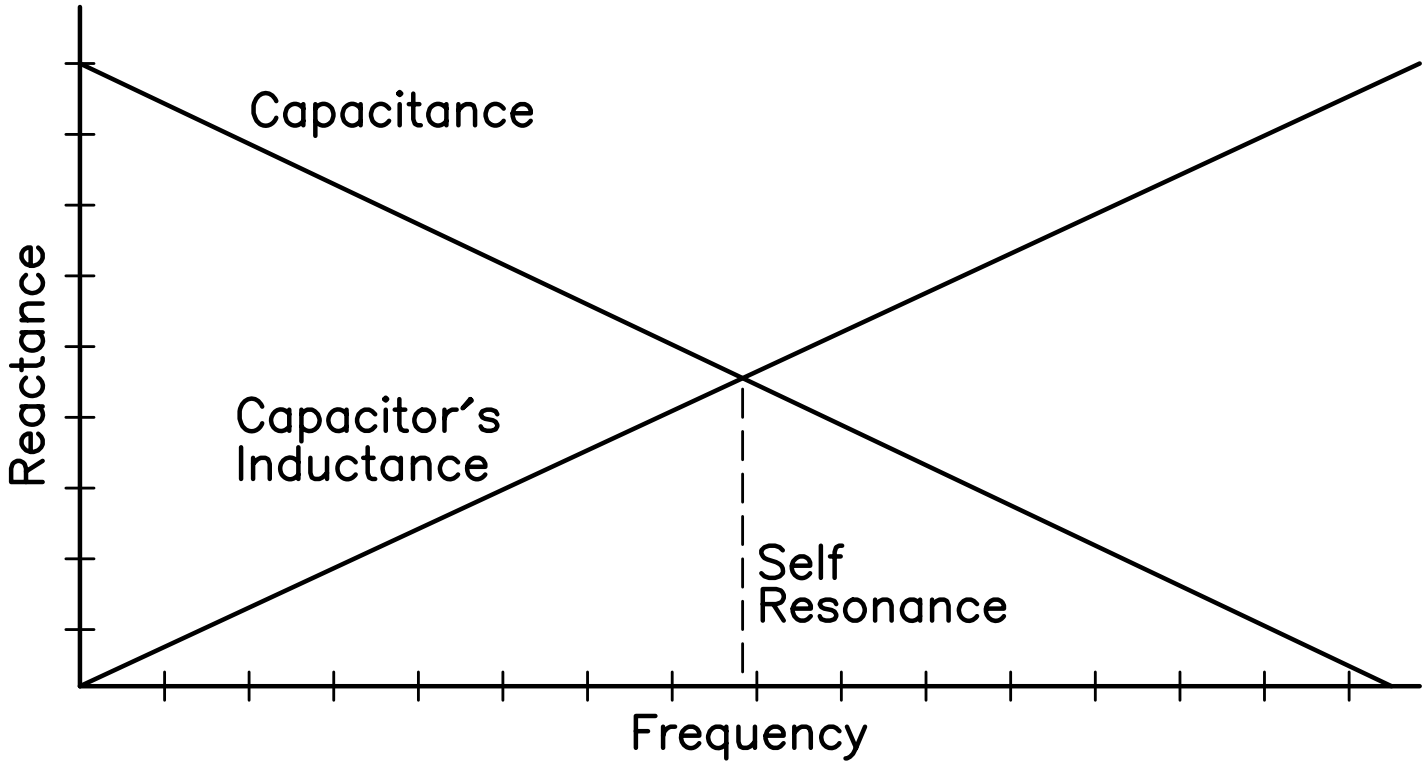
Decoupling - Power Distribution System

- Capacitor's ability to provide Energy is a function of Caps Reactance (Z) vs. Frequency -



Capacitor's Impedance vs. Frequency.

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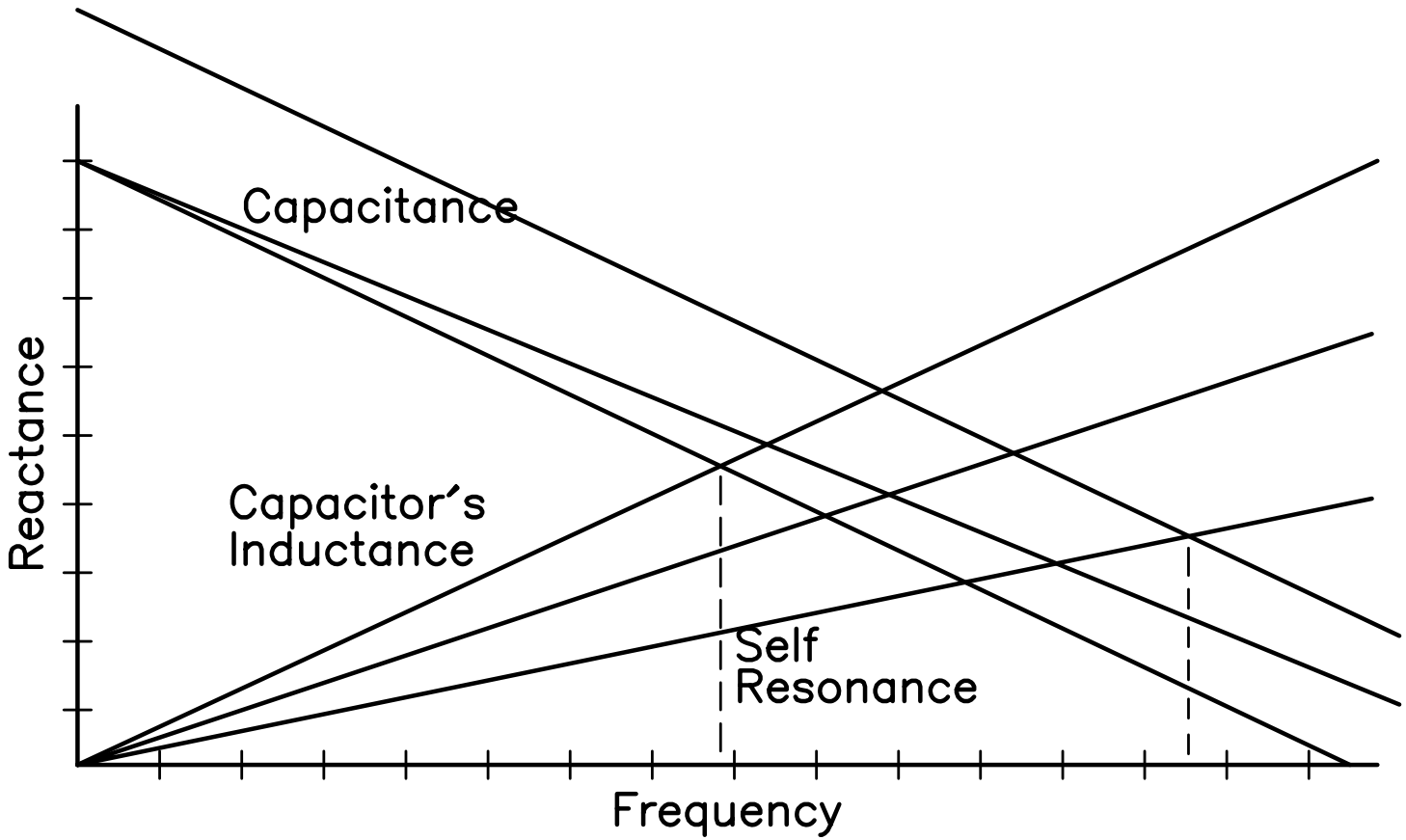
Decoupling - Power Distribution System



Capacitor's Impedance vs. Frequency.

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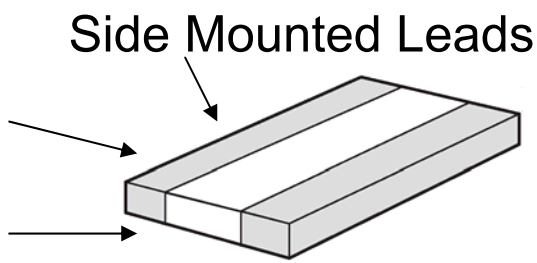
Decoupling - Power Distribution System

Cap Lead Frame Inductance (Per AVX):

Axial Lead -	2000 pH
1206 SMD -	1250 pH
0805 SMD -	1050 pH
1210 SMD -	980 pH
0603 SMD -	870 pH
0402 SMD -	650 pH
0612 SMD -	610 pH
0508 SMD -	600 pH
16 pin BGA-	50 pH



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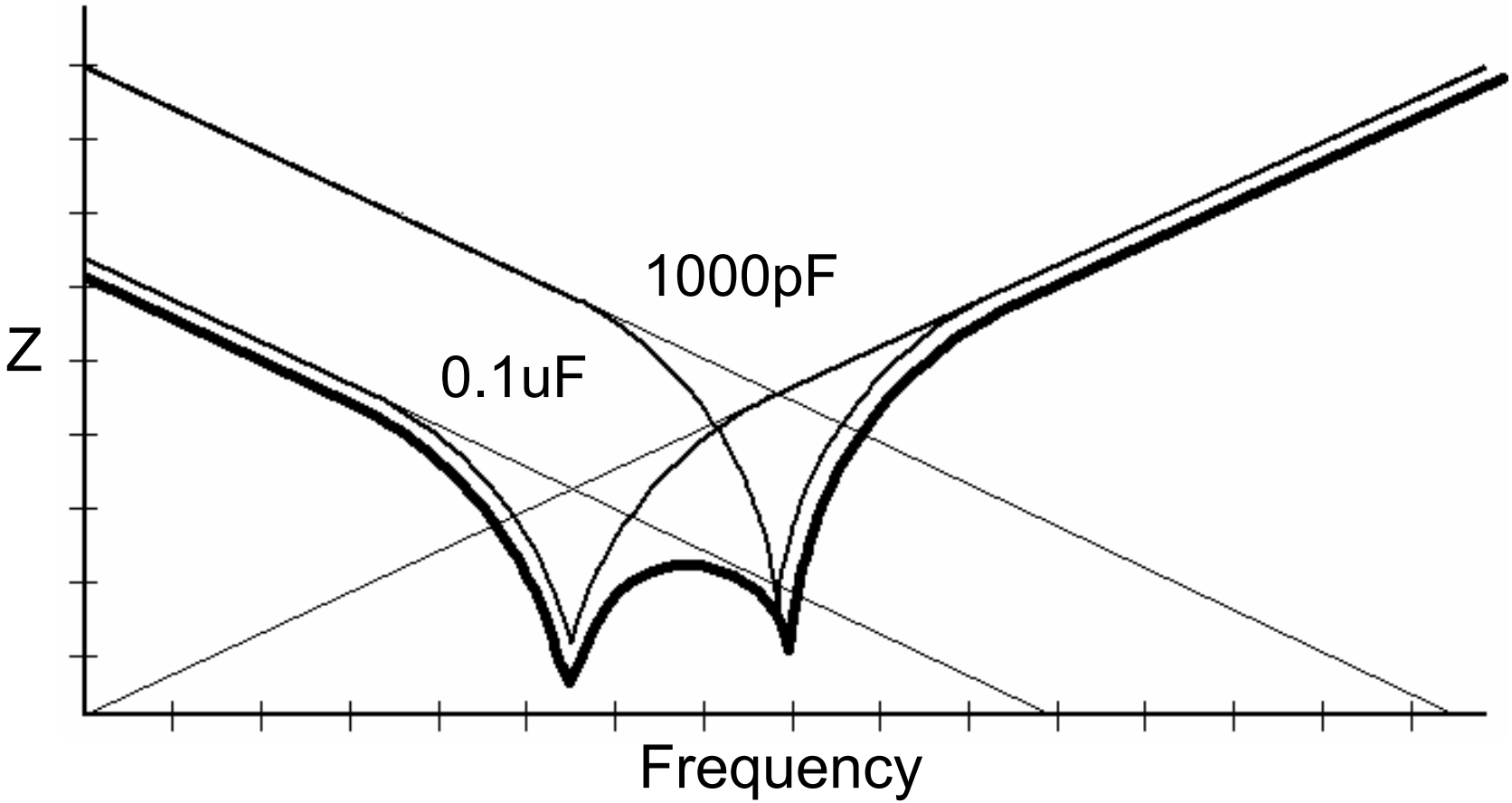
Decoupling - Power Distribution System



Intended Goal of Two Parallel Capacitors.

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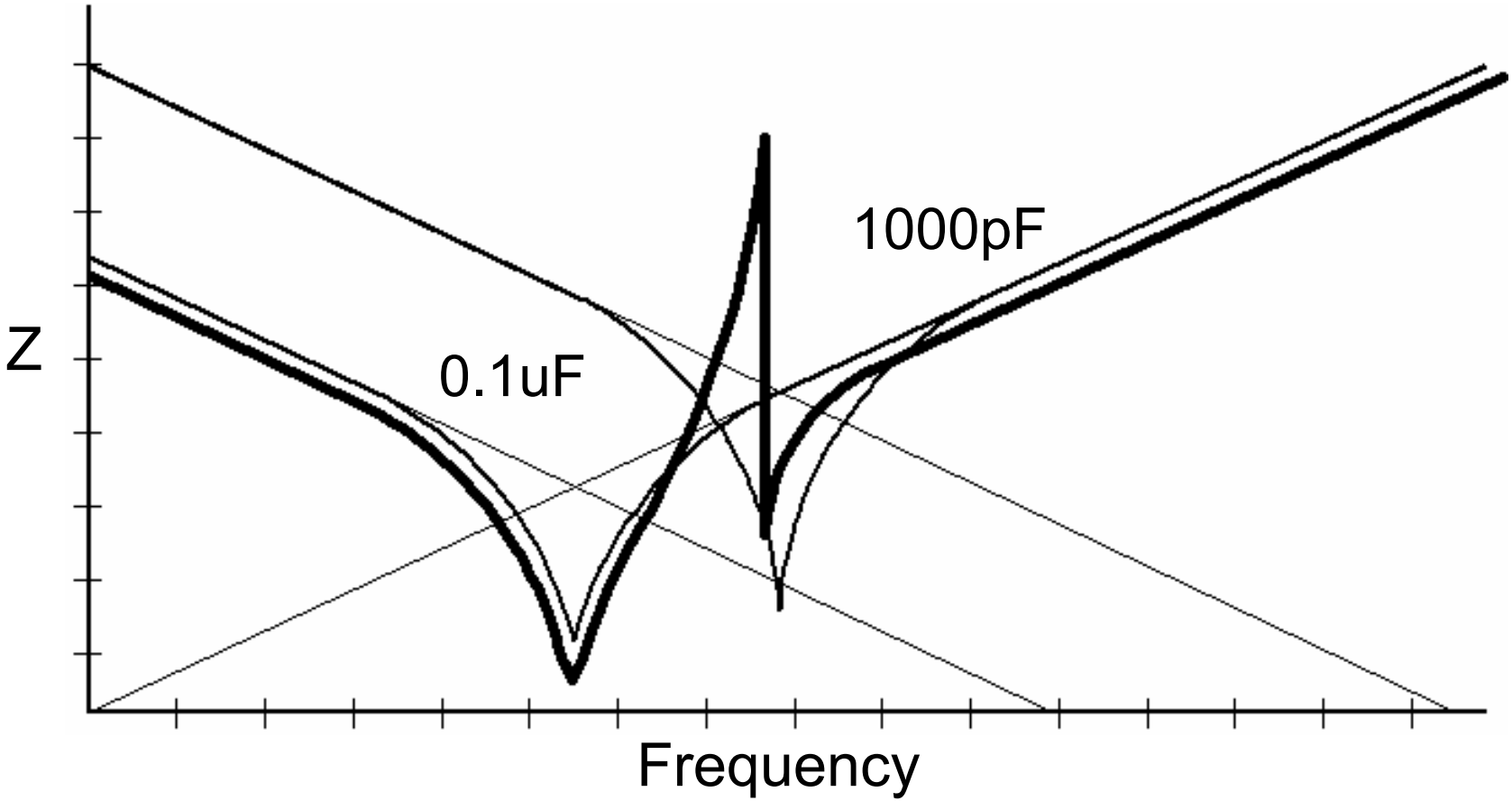
Decoupling - Power Distribution System



This is what REALLY Happens!!!

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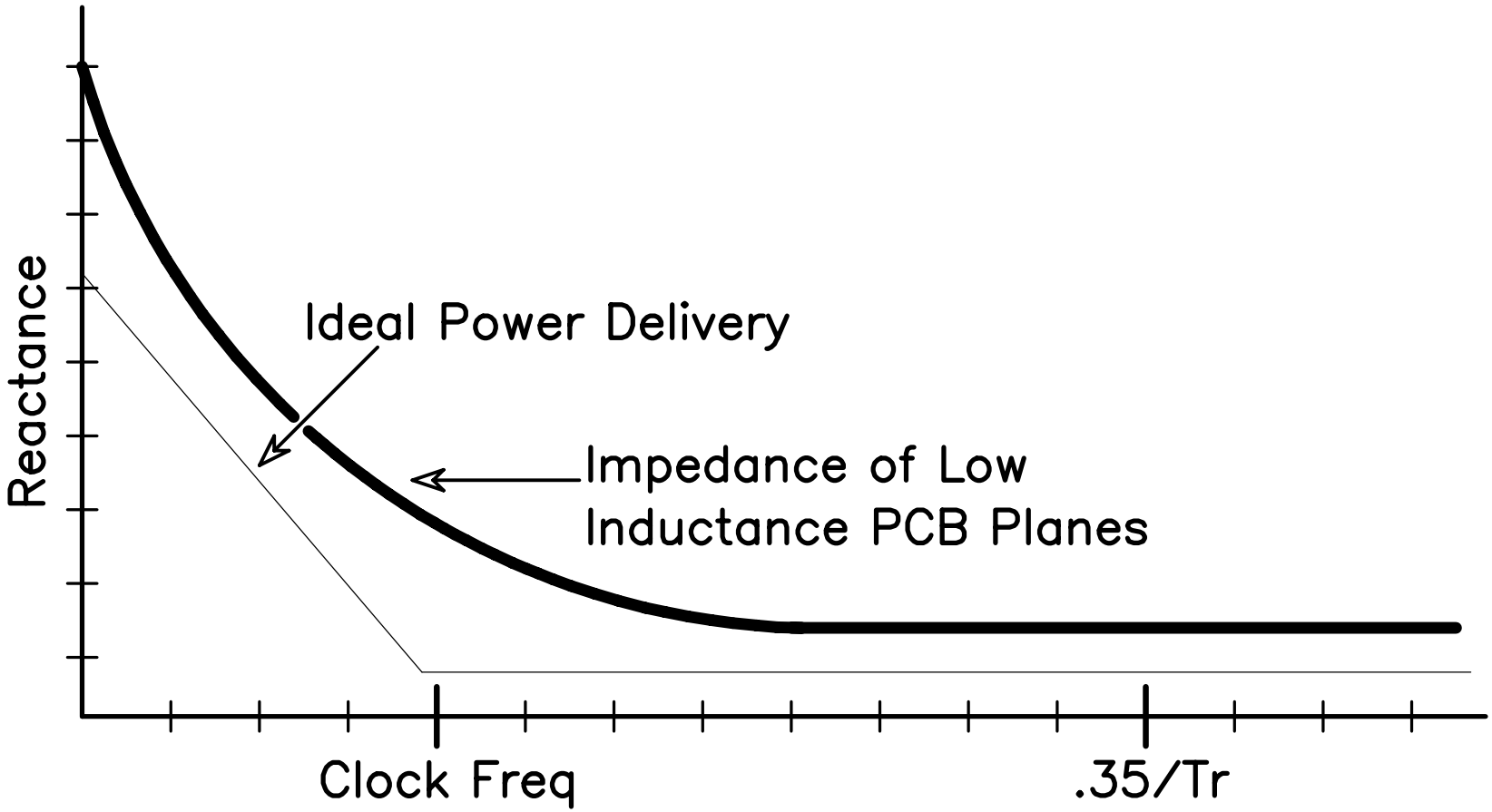
Decoupling - Power Distribution System



Planes alone Often don't have adequate Capacity.

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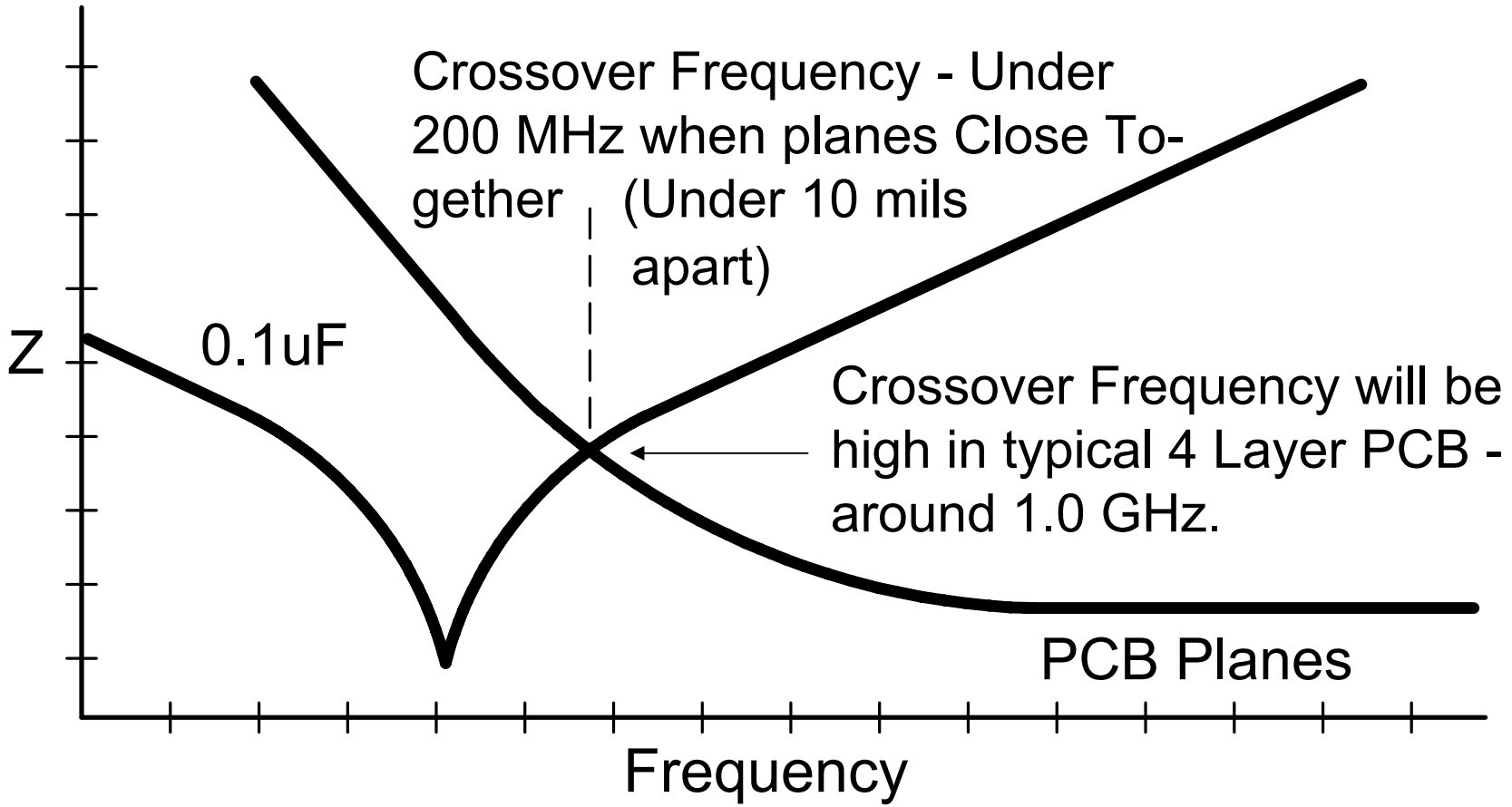
Decoupling - Power Distribution System



Optimum Solution in Typical PC board.

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Decoupling - Power Distribution System

TI's 'Opinion' on Decoupling

Texas Instruments
www.ti.com

Practical PCB Design Rules

TI's App Note is correct for 2 Layer & conventional 4 layer Boards.

Many research papers explain why 'NOT' to use the bottom structure on 6 layers and up.

Figure 12. Poor and Good Placement and Routing of Bypass Capacitors

- **Think about the importance of connecting the planes to the IC through a Low Inductance path, then ponder whether TI's Strategy is better???**

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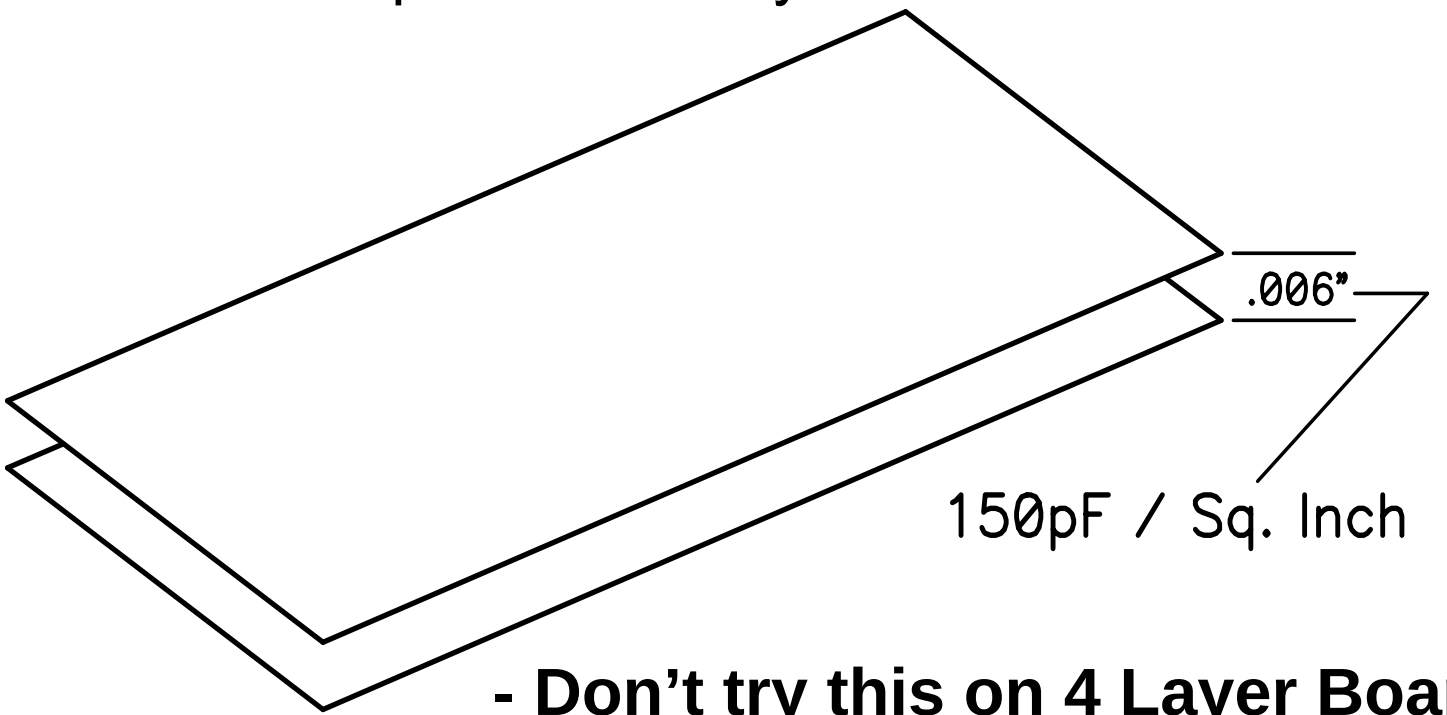
Decoupling - Power Distribution System

Power and Ground Planes

.003” to .006” Spacing creates a Large Plate Capacitor of Very Low Inductance.



- Don’t try this on 4 Layer Boards -

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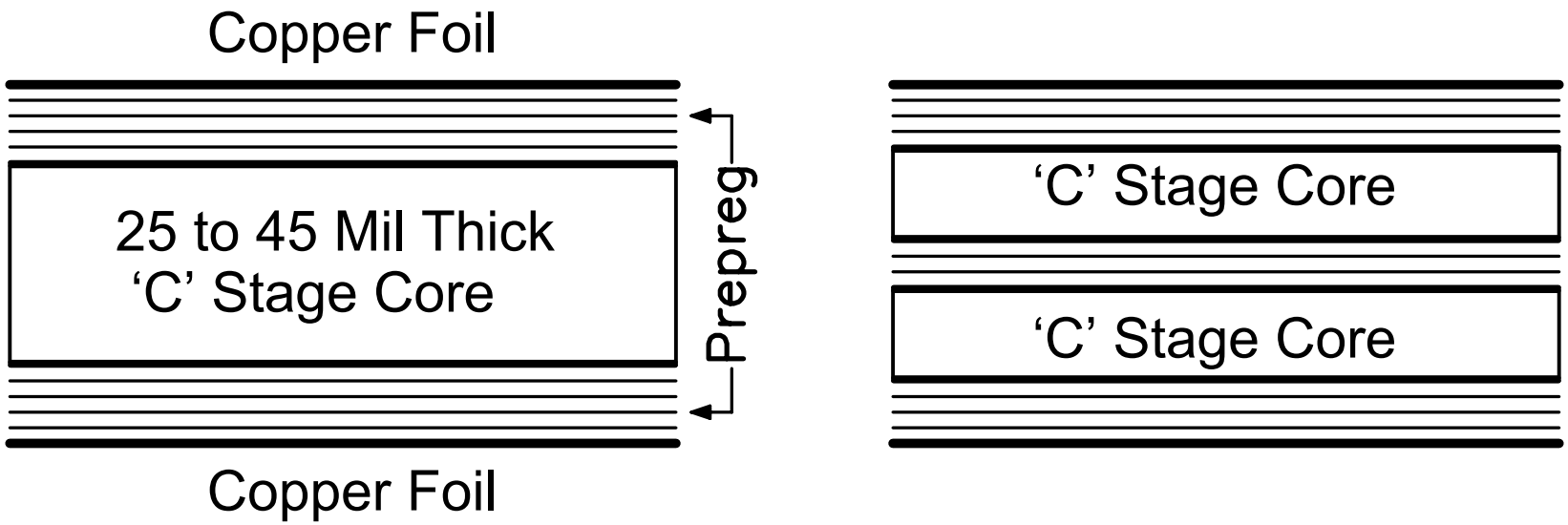
Decoupling - Power Distribution System



Most PC Boards are "Foil Laminated"

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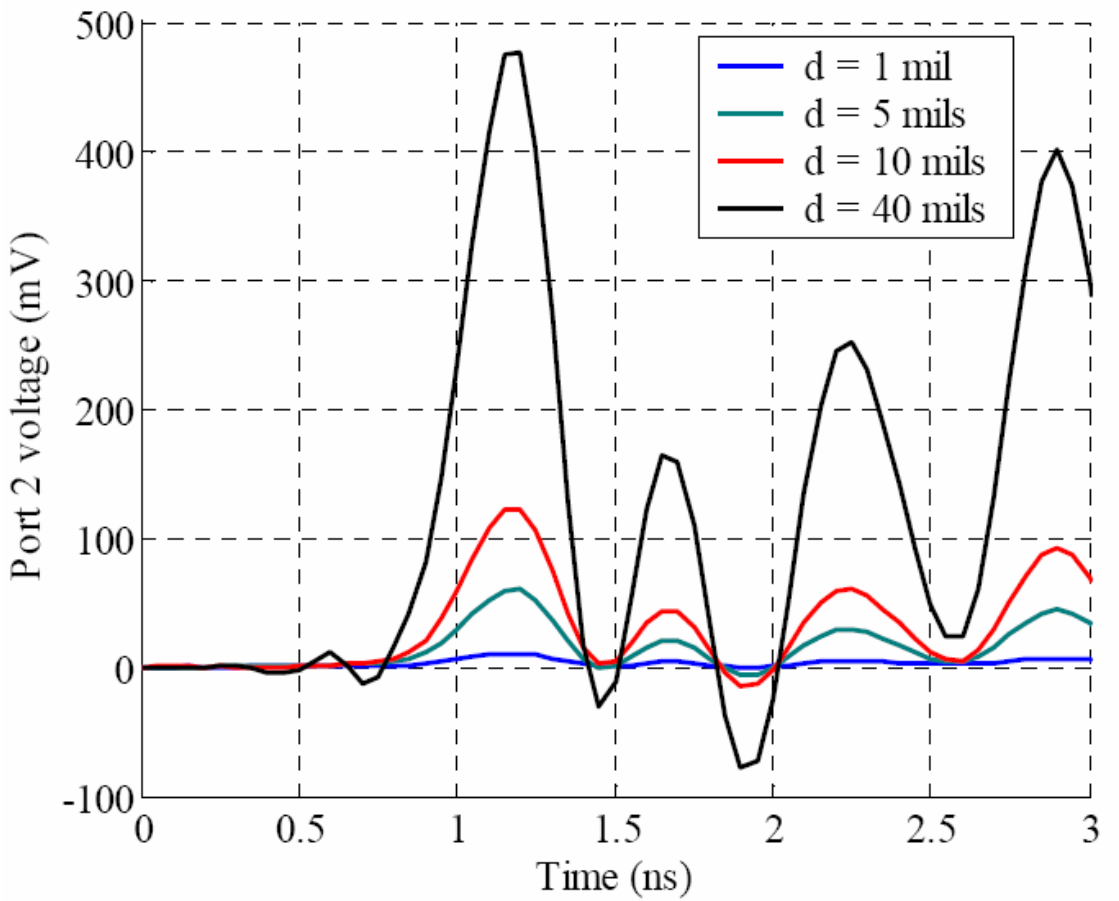
Decoupling - Power Distribution System

- Power Bus Switching Noise relative to spacing between Power and Ground.



(Source: University of Missouri at Rolla)

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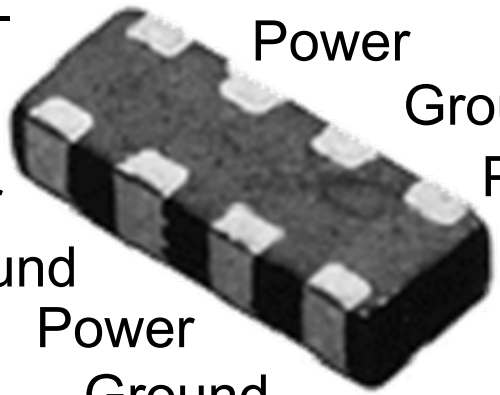
Decoupling - Power Distribution System

Array



X2Y Cap

1206 x 4 - 70 pH*

0603 - 50 pH*

(* when connected per manufacturer's recommended via structure)

- Multistage, Multipin Capacitors -

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EMI- Coupling Mechanism Control

Positions of Components -

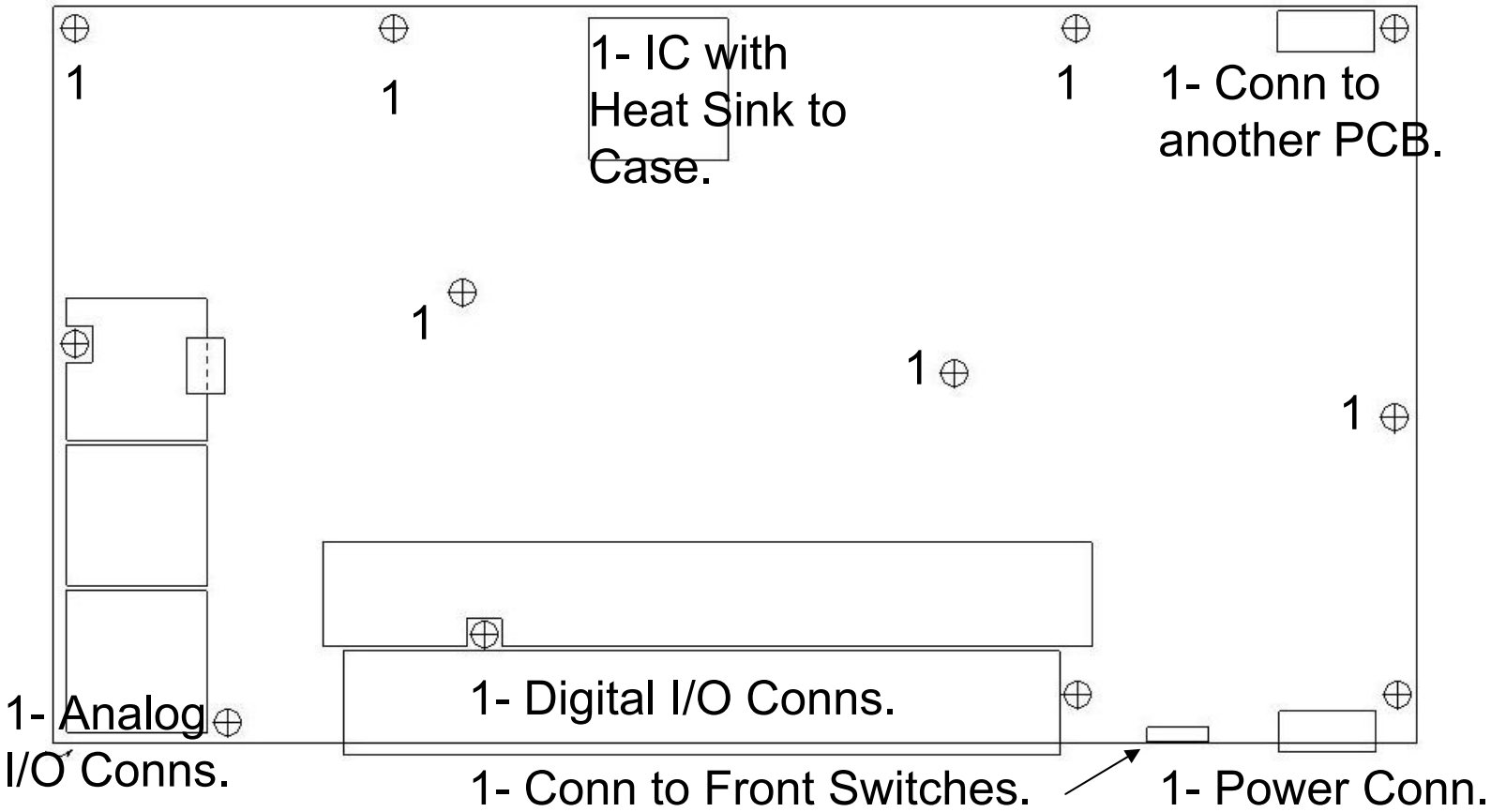
- Group Components by Function / Family.
  - Analog and Digital Devices in own areas.
  - Devices Operating at Different Voltages.
  - Devices at Different Frequencies.
  - By Function within a Given Family or Voltage.
  - All ICs routing to Connectors MUST be placed Very Close to their respective connector.

Approximate order of Parts Placement

1) Parts Fixed by mechanical design.
   - Mounting Holes.
   - I/O connectors.
   - ICs mounted to Heat Sinks that Attach to unit Chassis.
   - Any other Semi-Fixed components.

Exact position of these MUST be Negotiable (can be tweaked slightly to accommodate components on very dense designs).

EMI- Coupling Mechanism Control



Items Fixed by the Mechanical Design

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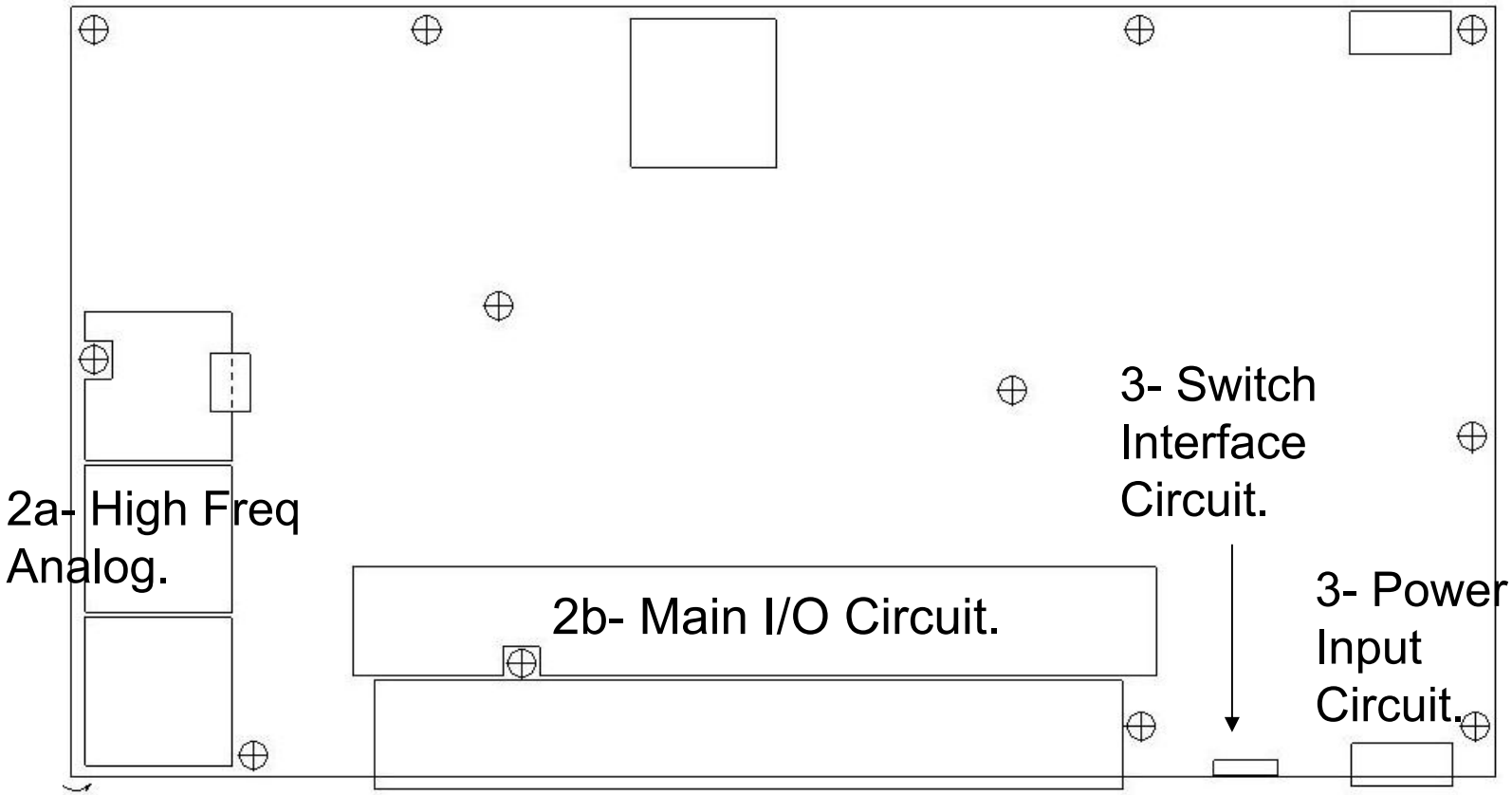
Approximate order of Parts Placement

2) Parts in Main I/O sections (EMI concern) -
   - I/O Parts Grouped AT the I/O connectors.
   - Analog Section(s) get Priority.

3) Components with inputs or outputs that route off the board, through a power cable, signal cable within unit, cable to front panel switches, etc. (EMI Concern) -
   - I/O Parts Grouped AT or VERY Near the 'Off Board' connector.

EMI- Coupling Mechanism Control



Components Routing to the I/O

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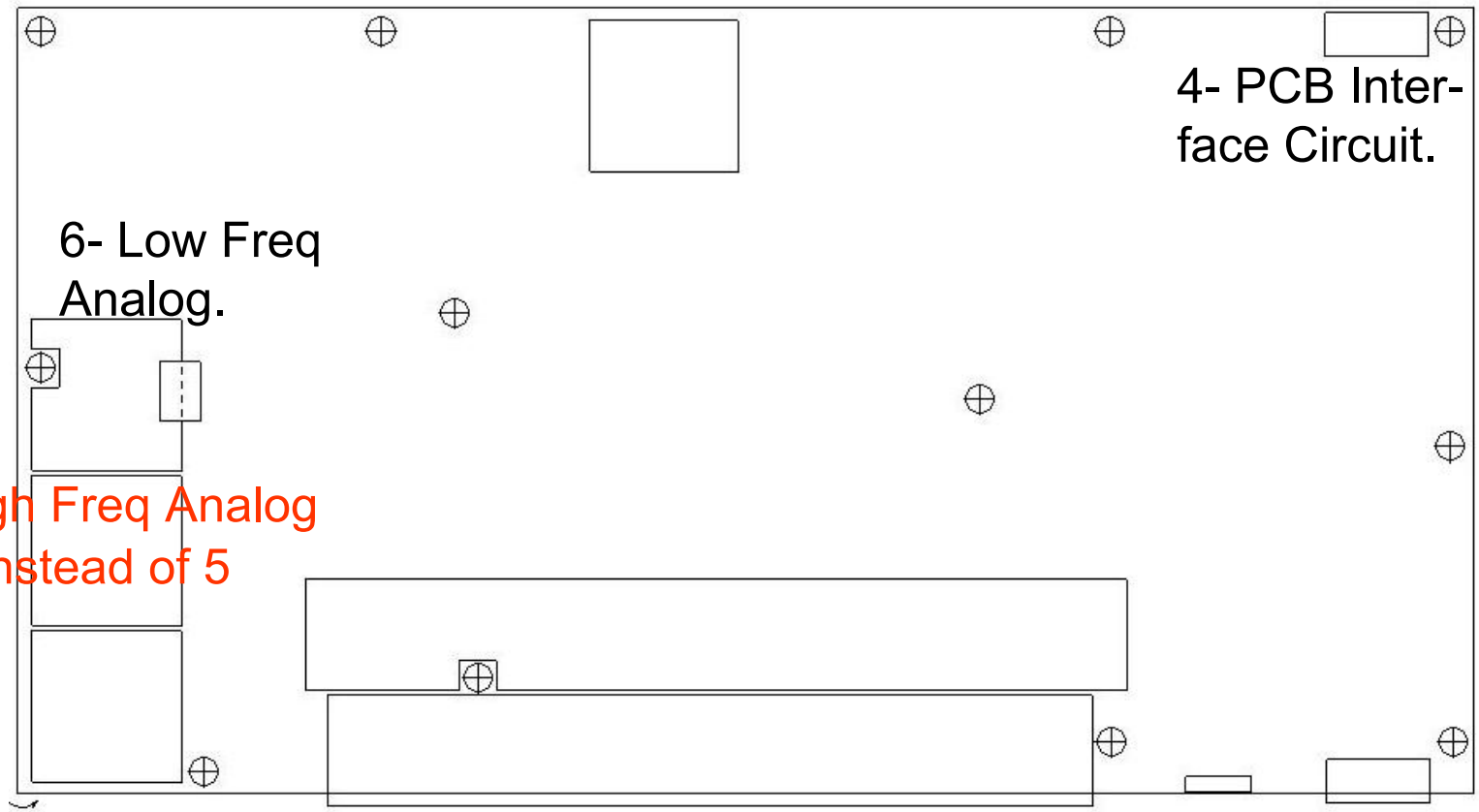
Approximate order of Parts Placement

4) Components with inputs or outputs that route off Board, through Board-to-Board Connectors. (EMI / Signal Integrity Concern)-
   - I/O Parts Grouped AT or Very Near the 'Off Board' connector
5) High Frequency Analog (in its own section).
6) Low Frequency Analog (in its own section).
   - Be aware of Ground currents at Low Freq.

(**5 or 6 become #2 if they go to I/O Connector)**

EMI- Coupling Mechanism Control



Board-to-Board and Analog Ckts

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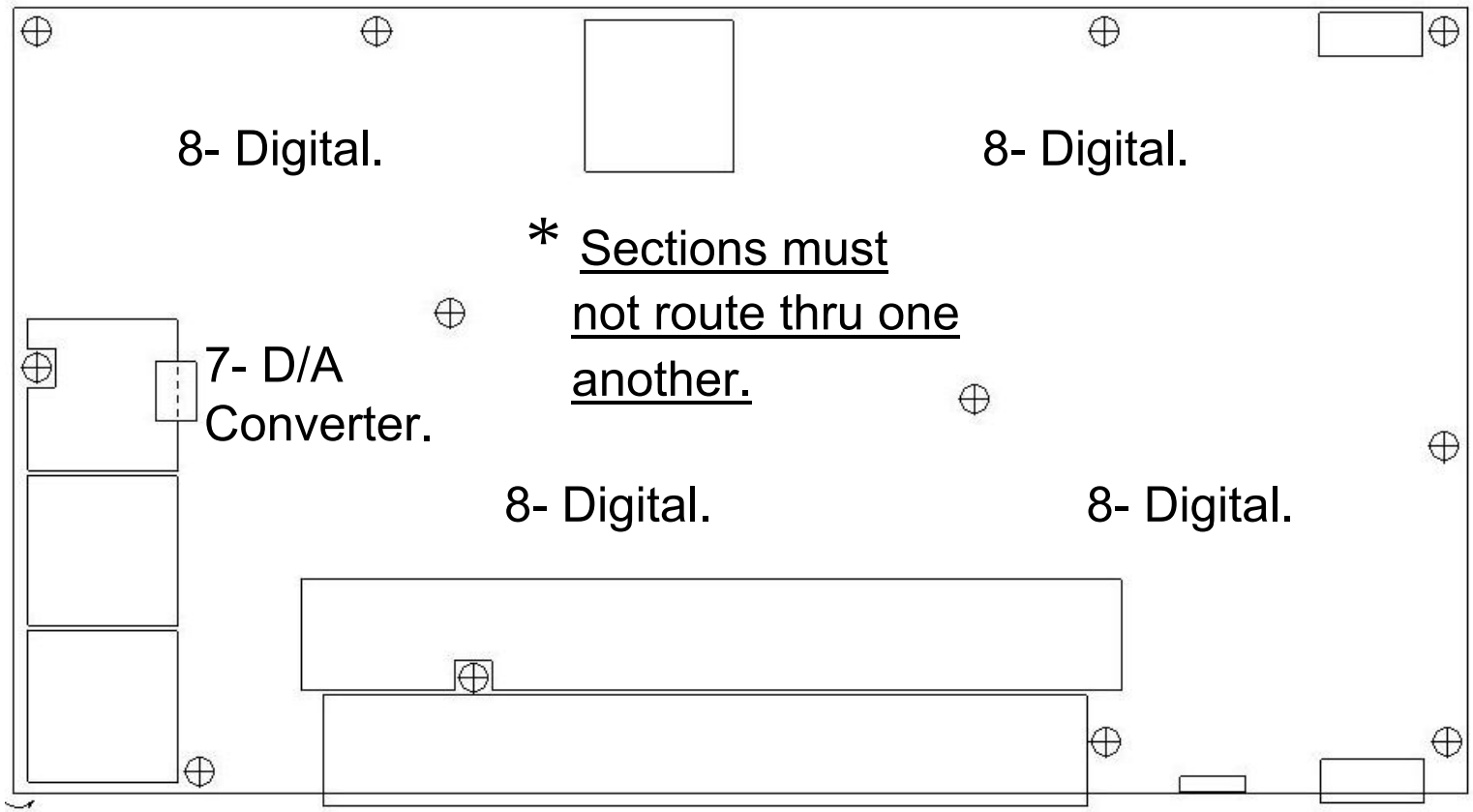
Approximate order of Parts Placement

7) Analog to Digital Interface -
   - A/D(s) and D/A(s) AT the Ana/Dig Junction.

8) Digital section(s).
   - Highest Speed Areas and Nets first.
   - 5V, 3.3V, etc components in Own Areas.

***Sections MUST be placed so routes from section to section do not cross through sections to which they DO NOT belong.**

EMI- Coupling Mechanism Control



A/Ds or D/As and Digital Sections

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Position of Planes -

- Once Parts are in Own Geographic Areas:
  - Structure Power/Gnd Planes under each area.
  - Based on Supply Voltage for that section.
  - Align Gnd Plane for each Voltage to Match Shape of Power Plane. (**IF Gnd Plane to be Split**)

- Analog & Digital Ground Planes Connect at Point (or Points) in Common.
  (ie- A/D or D/A Converter)

Signal Route Positions -

- Once Board is divided Geographically:
  - Only Signals Common to Both Areas Route between the Areas.
  - Those Signals Cross Only at Point(s) of Common Ground.
  - All other Signals Must remain in Own Geographic Area and NOT cross Gaps in Planes.

EMI- Coupling Mechanism Control

Ground Plane Split -

- Do we NEED or WANT to Split Ground Plane in a Circuit (A/D, 3v/5v, etc.)?

- Decision is Primarily a Function of-
  - Frequency.
  - Position of Circuit Components.
  - Position of Signal Routes.

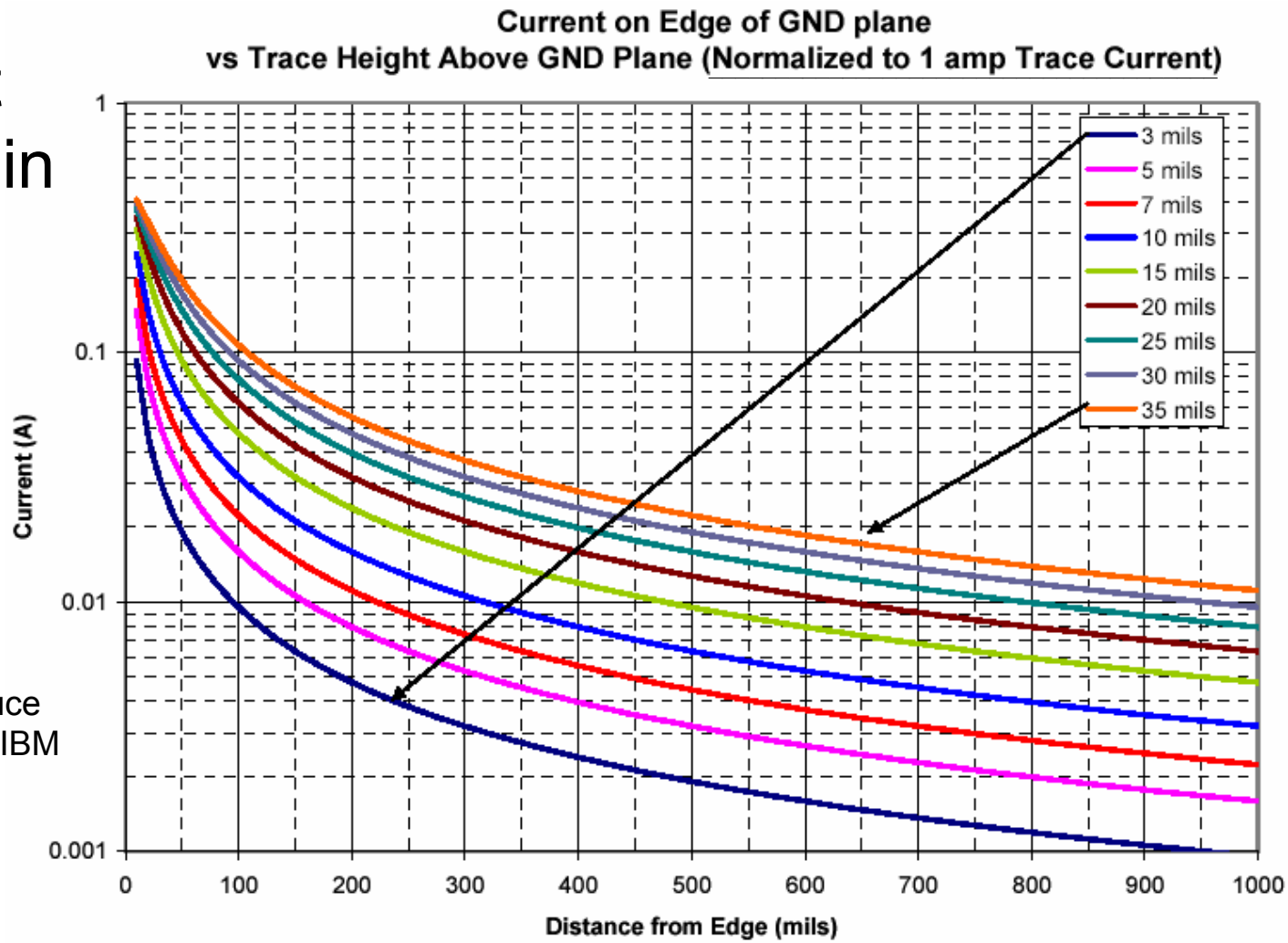
EMI- Coupling Mechanism Control

Ground Plane Split may be Necessary if -

- Once Analog and Digital Sections are TOO close to one another, **AND** -
- The analog section has extreme sensitivity
  - ie - -100+ dBm (1 - 2 microvolts), **AND** -
- Fast digital signals are routed close to and in Parallel with analog to digital interface.
- This only happens with 18+ bit A/D (or DAC) or in TX / RX circuits like cell phones.

EMI- Coupling Mechanism Control

Current spread in ground plane -



Source - Dr. Bruce Archambeault - IBM

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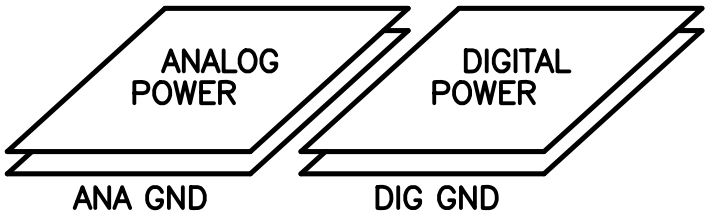
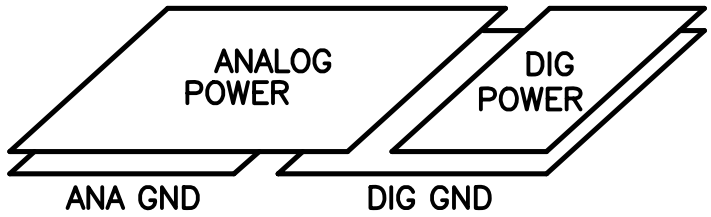
EMI- Coupling Mechanism Control

Position of Planes -



Proper Plane Alignment



Trouble Brewing

Correct Power and Ground Plane Alignment (When Splitting Gnd)

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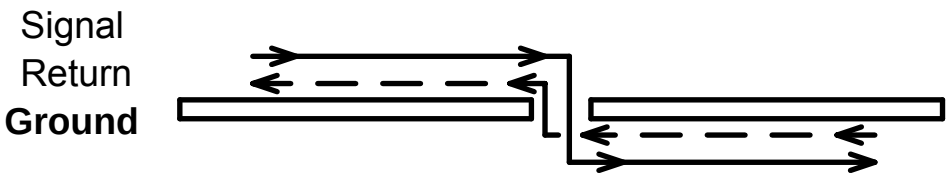
EMI- Coupling Mechanism Control

Islands in Planes -

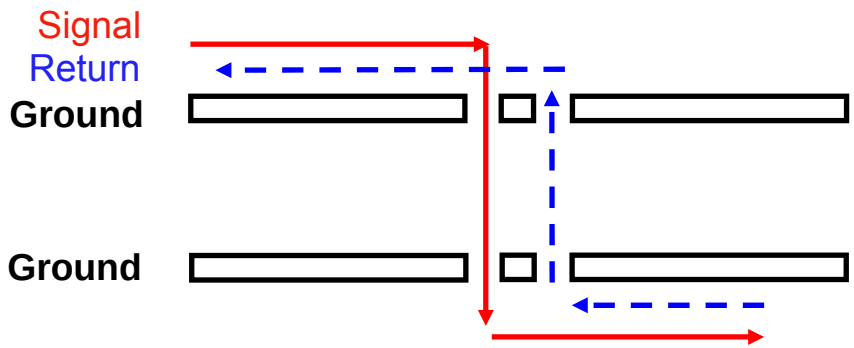
- Recommendation of IC companies-
  - If Noise Coupling to Sensitive IC(s) thru Power Plane is potential problem, segment Planes (make Island) under that IC.
- Connect Main Power/Gnd to Island -
  - Through Single Point, located away from Noisy Sections of Main Planes (**or**)
  - Through Ferrite(s) or Low Value Resistor(s) or Low Pass Filter(s).
- Should we Isolate Ground as well?

Additional Routing Details -

- When moving signals between layers, route on either side of the same plane, as much as possible!!!



- When moving signals between 2 different planes, use a transfer via VERY near the signal via.



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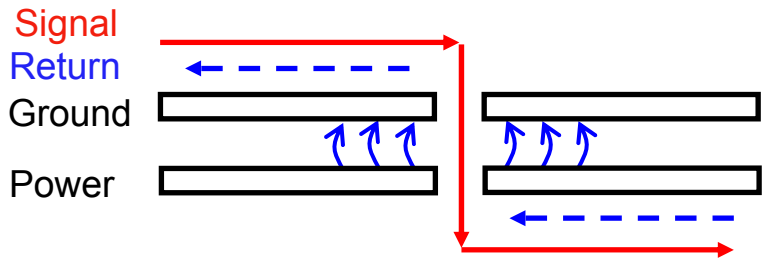
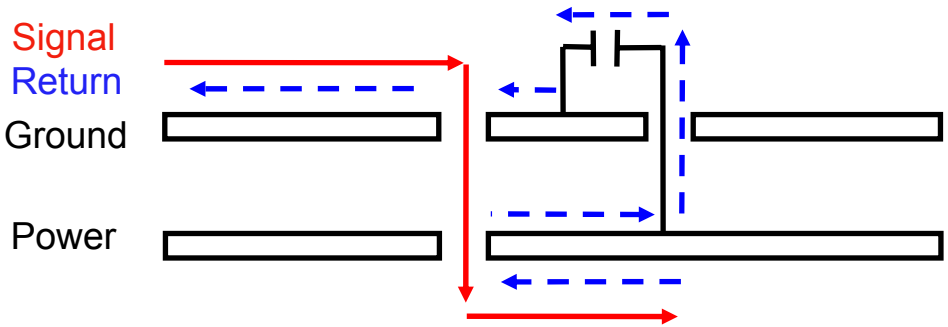
Additional Routing Details -

- When routing signals from Power to Ground, Return energy will transfer as follows -



Tightly Coupled Planes



Loosely Coupled Planes w/ Cap???

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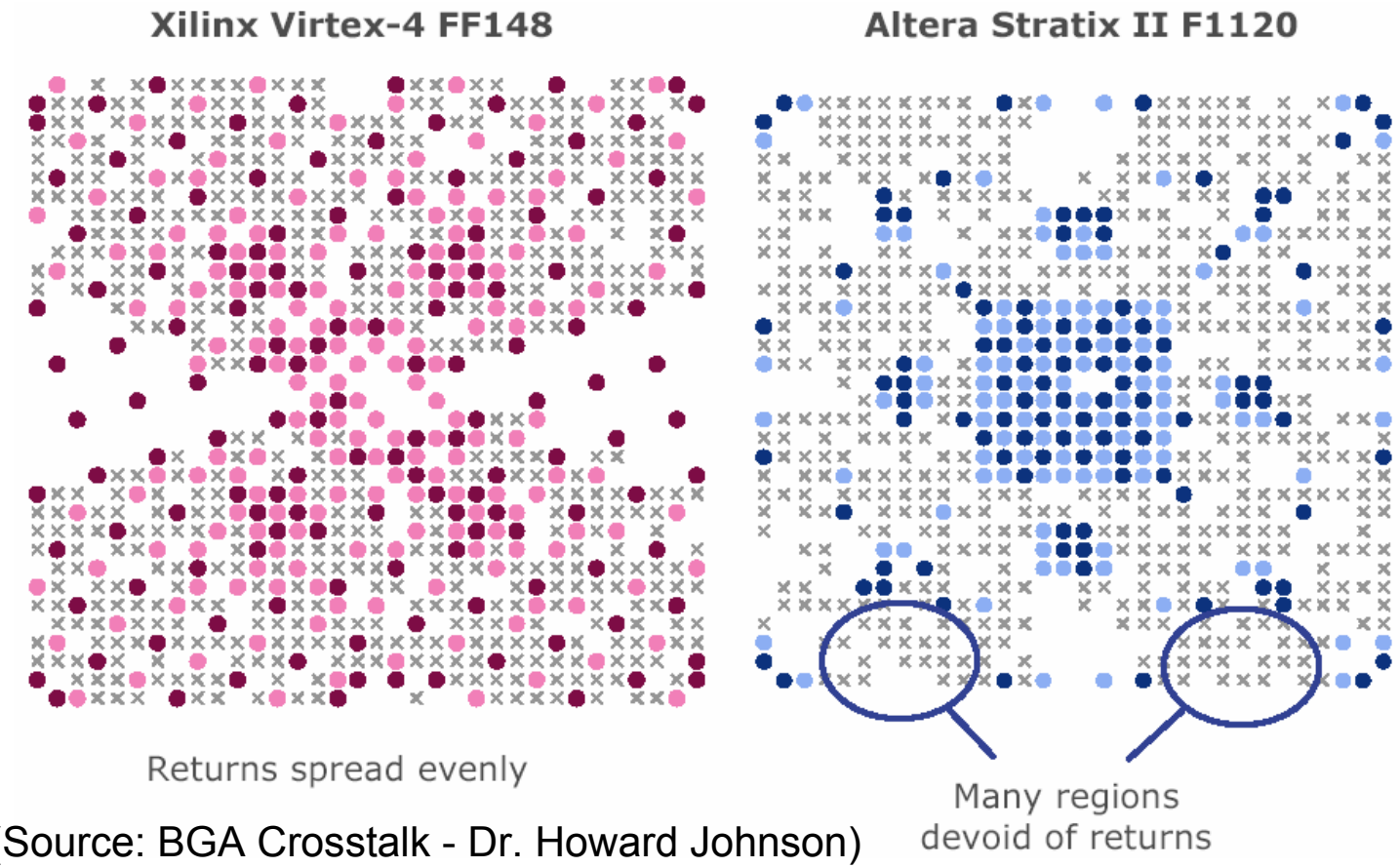
EMI- Coupling Mechanism Control

Impact of Lead Frame on signal noise, switching noise and Vcc/Ground Bounce

F1120 had 5X greater noise level than FF1148 -



(Source: BGA Crosstalk - Dr. Howard Johnson)

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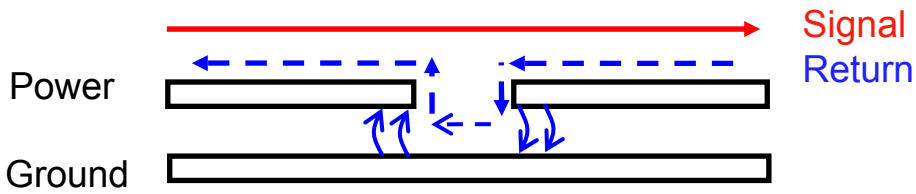
Additional Routing Details -



- With a second, un-split plane, TIGHTLY coupled (<.008”) to the split plane, the return energy can capacitvely couple from the split plane to the whole plane and back again.
- **If both planes of a pair are split, don’t cross at ANY frequency.**

PC Board Layer Stacking

- Goals for PC Board Structure:
  - Can be Fabricated in a Balanced fashion.

  - Can be Fabricated in a Balanced fashion.
  - Place Power and Ground where they can do Most Good.
  - Maintain Electrically Quiet Circuit, by placing layers to achieve layer Pair Routing.

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PC Board Layer Stacking

- Since Decoupling Capacitors cannot provide energy above 150 MHz (at Best), Energy for Fast Switching edges is drawn from the capacitance formed by the parallel plates of the power planes in the PCB.
- Many PCBs do not have sufficient power plane area to create a capacitor large enough to supply the switching currents required.
- The result is excessive high frequency ripple on the power planes and associated high EMI.

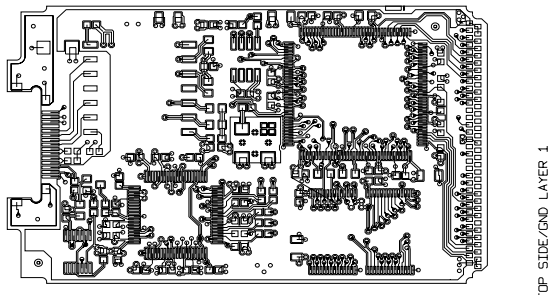
(Info largely from Speeding Edge, Spring 2001)

PC Board Layer Stacking

- Most PCBs have significant unused spaces on Signal Layers.
- This unused area can be Filled with Copper to provide Additional Plate area to increase the size of this capacitor.
- Copper fill areas must be tied to the appropriate voltage using component power leads or single pin parts with the appropriate designation. (Use vias to do the tie.)

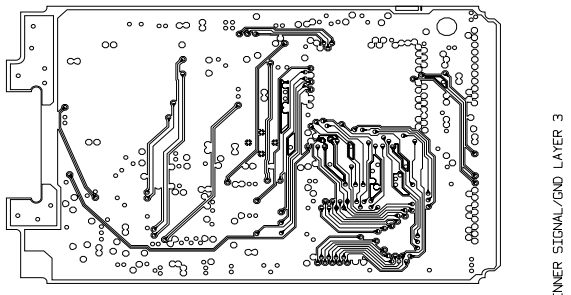
(Info largely from Speeding Edge, Spring 2001)

PC Board Layer Stacking

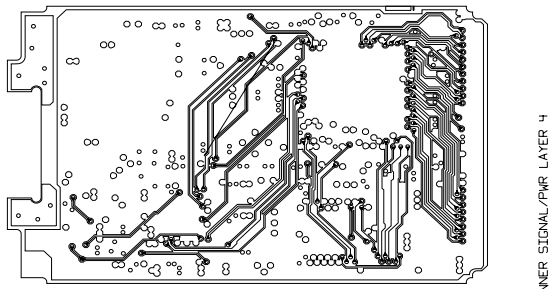


LAYER 1, SIGNAL FILLED WITH GROUND

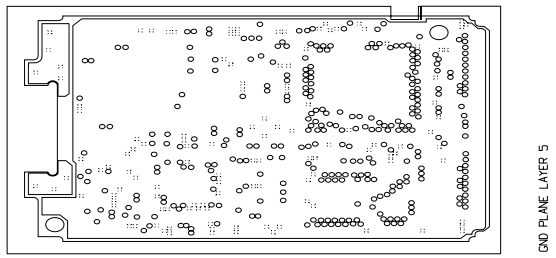
LAYER 2, Vcc LAYER



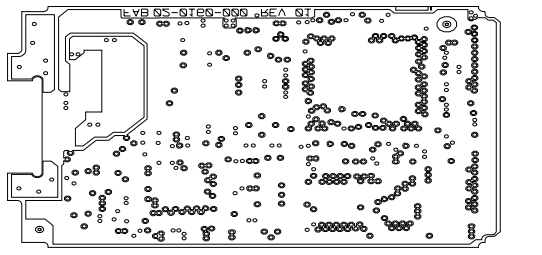
LAYER 3, SIGNAL FILLED WITH GROUND



LAYER 4, SIGNAL FILLED WITH Vcc



LAYER 5, GROUND LAYER



LAYER 6, SIGNAL FILLED WITH Vcc

Power plane capacitance without fill, 500 pF. with fill 4100 pF.

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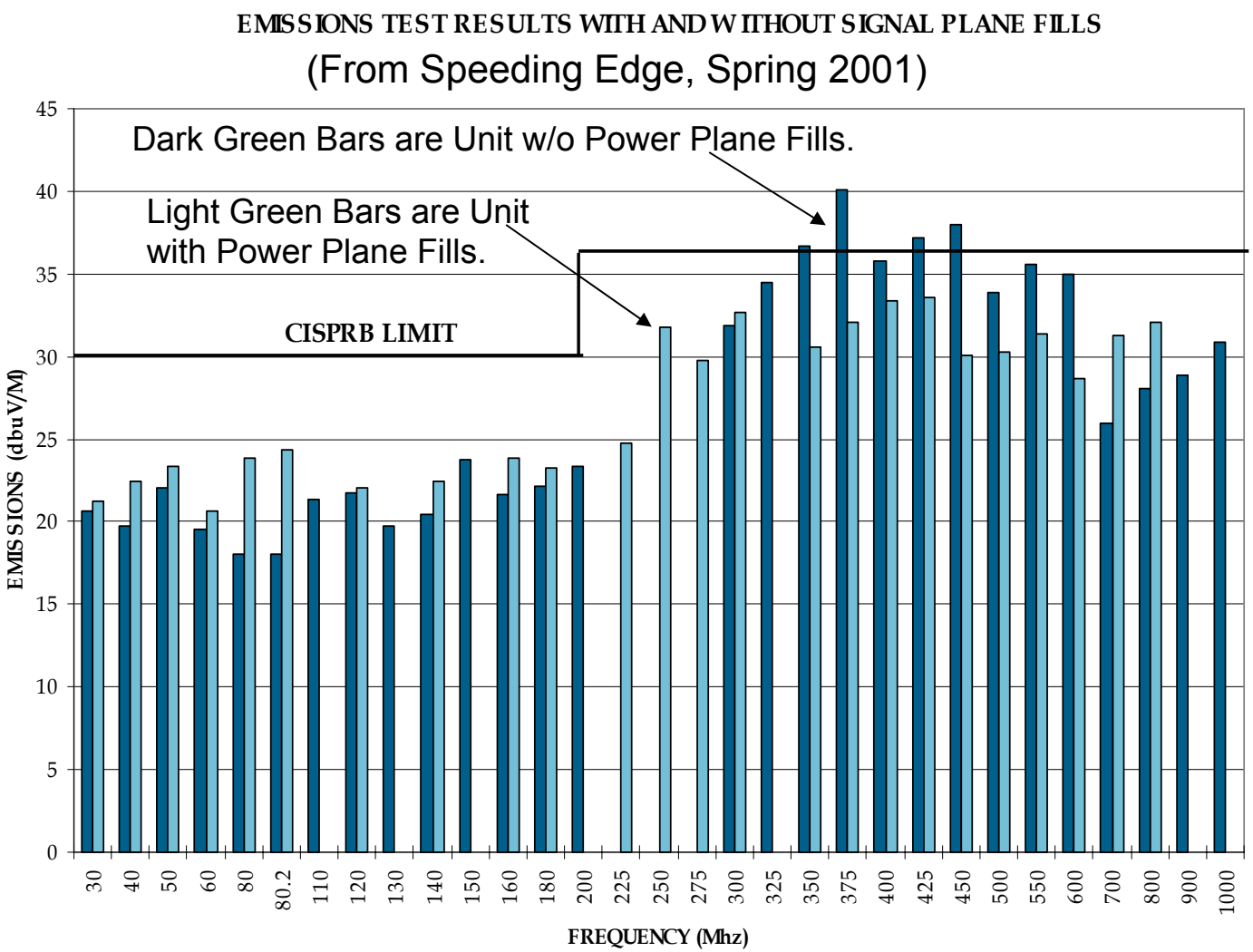
PC Board Layer Stacking



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PC Board Layer Stacking

Four(4) Layer Designs

(A)
----Ground-----
----Sig/Pwr-----

----Sig/Pwr-----
----Ground-----

(B)
---Sig/Poured Pwr---
--------Ground---------

--------Ground---------
---Sig/Poured Pwr---

PC Board Layer Stacking

Six(6) Layer Designs

-----Power------	----Sig/Pwr----
----Sig/Gnd-----	----Ground-----
-----Power------	----Sig/Pwr----
----Ground------	----Ground-----
----Sig/Pwr-----	-----Power------
----Ground------	----Sig/Gnd----

Six(6) Layer Designs to AVOID

-----Signal------	-----Signal-----
-----Signal------	-----Power-----
----Ground------	-----Signal------
-----Power------	-----Signal------
-----Signal------	----Ground-----
-----Signal------	-----Signal------

PC Board Layer Stacking

Six(6) Layer Designs

-Short Sig/Pwr-	----Sig/Pwr-----
----Sig/Gnd-----	----Ground-----
-----Power------	----Sig/Pwr-----
----Ground------	----Sig/Gnd-----
----Sig/Pwr-----	-----Power------
-Short Sig/Gnd-	----Sig/Gnd-----

PC Board Layer Stacking

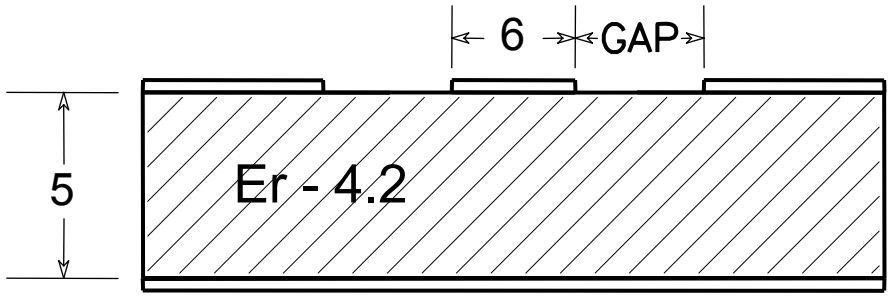
Eight(8) Layer Designs

----Signal-----	---Sig/Pwr----
---Ground-----	---Ground-----
----Signal-----	---Sig/Pwr----
----Power-----	---Ground-----
---Ground-----	----Power-----
----Signal-----	---Sig/Gnd----
---Ground-----	----Power-----
----Signal-----	---Sig/Gnd----

Eight(8) Layer Designs to AVOID

----Signal-----	----Signal-----	----Signal-----
----Signal-----	----Signal-----	----Power-----
----Signal-----	----Power-----	----Signal-----
----Power-----	----Signal-----	----Signal-----
---Ground----	----Signal-----	----Signal-----
----Signal-----	---Ground-----	----Signal-----
----Signal-----	----Signal------	---Ground-----
----Signal-----	----Signal------	----Signal-----

Effect of Co-Planar Copper Pour



Gap vs Impedance **(w/Soldermask)**

Gap (mils)	Impedance	Gap (mils)	Impedance
5	45	11	51
6	47	12	52
7	49	13	52
- 8	50	14	52
9	50	15	52
10	51	No Co-PI CU	53

PC Board Layer Stacking

- Basics:
  - Signal Layers placed One Dielectric Layer away from Plane gives Best Control of Impedance.
  - Outer Layers have Poorest Impedance Control and Poorest Cross Talk Control.
  - Plane Pairs give Highest Interplane Capacitance (Critical for EMI). Use Copper Pour!!!